MEASURING SUPPLY CURRENTS IN PRINTED CIRCUIT BOARDS

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I certify that I have read this thesis and that in my opinion it is fully adequate, in scope and quality, as a dissertation for the degree of Doctor of Philosophy

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Abstract

To realize the full performance potential of CMOS integrated circuits, the power networks supplying them must supply sufficient current, both transient and steady state, so that on-chip supply voltages remain within specified bounds. MOS transistor scaling has resulted in decreased supply voltages and increased circuit density. Since total power dissipation has remained unchanged or even increased, the combined result is a large increase in supply current and its time rate of change, making the design of power networks increasingly difficult. Measurements of voltages and currents in power networks are required to develop good design and simulation practices and to diagnose problems that arise in real systems.

This thesis presents a method that enables transient supply currents to be measured at the package to printed circuit board interface. The approach measures the magnetic fields generated by current carrying conductors. A simple induction loop is used to measure the magnetic fields. We demonstrate that such a device can be made small enough to measure PCB vias on 1 mm spacing, have a measurement bandwidth of 2 GHz, and can detect repetitive current changes as small as 6 μA/ns. This sensitivity is sufficient to detect supply current fluctuations in real printed circuit boards. Finally the method is applied to investigate the power network behavior for a large integrated circuit.

Acknowledgements

Without the help and encouragement of many people, completing this thesis would not have been possible. Above all, I want to thank my family, particularly my wife Cheryl, for their support. Their steady encouragement, patience and willingness to listen were providential. I also owe a debt of gratitude to Nick McKeown for setting me on the path that lead back to Stanford and, eventually, to this work.

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$\vec{\mathbf{B}}$	The magnetic field vector.
B	The magnitude of the magnetic field at a point in space.
C_{ox}	The unit area gate capacitance of an MOS transistor.
C	The velocity of light in a vacuum.
χ	Distance in the plane of an induction loop, normalized to the width of the loop: x/W.
D	The center to center spacing, or *pitch*, between two vias in a printed circuit board. Also, the unit spacing of a uniform two dimensional array of vias in a printed circuit board.
$d\vec{\mathbf{A}}$	The differential surface normal vector of an area.
δ_S	The skin depth of a conductor: the point at which the strengths of the electric and magnetic fields of an electromagnetic wave penetrating a conductor fall to one over the base of the natural logarithm.
δ	The via spacing normalized to induction loop width: D/W.
$\vec{\mathbf{E}}$	The electric field vector.
E_C	The electric field intensity at which velocity saturation occurs in an MOS transistor.
ε_r	The relative dielectric constant of a material.
f	The frequency of a signal or time varying quantity (e.g. voltage) in Hertz.
h	The height of an induction loop used to sense the time rate of change of magnetic flux linking its area.
I_{DSAT}	The drain current of an MOS transistor operating in saturation.
I	The current in an electric circuit.

$\mathbf{I_{cap}}$ The vector of printed circuit board bypass capacitor currents to be measured.

$\mathbf{I_{pin}}$ The vector of integrated circuit package pin currents to be measured.

$\mathbf{I_{plane}}$ The vector of currents contributed by the printed circuit board power plane to individual vias.

I_{via} The current passing through a printed circuit board via.

$\vec{\mathbf{J}}$ The current density field vector.

$\vec{\mathbf{J}}_{\mathbf{S}}$ The surface current density field vector.

L The inductance of an electric circuit.

ℓ The channel length of an MOS transistor.

M The mutual inductance between two circuits.

$\mathbf{M}$ The matrix of mutual inductances between multiply linked circuits.

μ The magnetic permeability of a material.

μ_o The magnetic permeability of a free space.

$\vec{\mathbf{P}}$ The Poynting vector, indicating the direction of propagation of an electromagnetic wave.

R The resistance of an electric circuit.

R_O The drain to source resistance of an MOS transistor.

ρ The resistivity of a material.

t_{pLH} The propagation time of a digital circuit when the output transitions from low to high.

t_{pHL} The propagation time of a digital circuit when the output transitions from high to low.

$\mathbf{V_{cap}}$ The vector of induction loop voltages induced by currents in bypass capacitors.

V_{DD} The supply voltage or voltage rail for CMOS circuits.

V_{DDQ} The supply voltage or voltage rail for output drivers of CMOS integrated circuits.

V_T The threshold voltage of an MOS transistor.

V_{fi} The voltage induced in an induction loop when the loop is fully inserted at a location of a printed circuit board.

V_{hi} The voltage induced in an induction loop when the loop is partially inserted at a location of a printed circuit board.

V_{out} The induced voltage in an induction loop used to sense the time rate of change of magnetic flux linking its area.

$\mathbf{V_{pin}}$ The vector of induction loop voltages induced by currents in the package pins of an integrated circuit.

v_{SAT} The carrier saturation velocity in the channel of an MOS transistor.

V_{SS} The source voltage or voltage rail (usually the ground reference) of CMOS circuits or integrated circuits.

V_{SSQ} The source voltage or voltage rail (usually the ground reference) of output drivers of CMOS circuits or integrated circuits.

V^* The normalizing induction voltage: $h\left(\frac{\mu_o}{4\pi}\right)\frac{\partial I}{\partial t}$

W The width of an induction loop used to sense the time rate of change of magnetic flux linking its area.

W_{mos} The channel width of an MOS transistor.

ω The angular frequency of a signal or time varying quantity (e.g. voltage) in radians per second.

ψ Distance normal to the plane of an induction loop, normalized to the width of the loop: y/W.

Chapter 1

Introduction

Over the last two decades, we have seen enormous progress in silicon technology. The drawn channel lengths of MOS transistors have fallen by over an order of magnitude from 1 μm to 65 nm, and 45 nm processes are in development. At the same time, improvements in silicon processing have reduced defect densities to the point where 1.5 cm square dies are commercially viable. The increase in performance of the resulting integrated circuits has been breathtaking. Single purpose devices have given way to large, multi-function devices, and entire systems on a chip are being investigated. The increase in operating speed has been equally impressive. Decreased CMOS circuit delays have allowed internal clock frequencies to increase from tens of Mega Hertz to several Giga Hertz. The resulting increase in performance has opened up entirely new applications for digital logic.

But this performance has come at a cost. The increase in circuit densities allows designers to place an ever larger number of circuits on a die, and the result has been ever greater complexity of the on-die system. At the same time, the combination of large die and advanced silicon processes has significantly increased the cost of bringing a new chip to market. It is not uncommon for the mask set for a large Application Specific Circuit, or ASIC, implemented in a modern CMOS process to cost many millions of dollars. Required times to market, however, have not decreased. The combination requires that large chips be correct by design. While significant progress has been made in circuit and system simulation and verification, the development of simulation tools to estimate dynamic power dissipation has lagged.

This leaves system designers without the necessary tools to ensure that their designs of power delivery networks are adequate. Their only recourse is to over-design these networks. This must change if the benefits of improved MOS technology are to be fully realized. Industry and the academy must collaborate to develop adequate dynamic power estimation tools.

As these tools are developed, there will be a need for experimentally measured data for their validation. Measurements of both voltage and currents in power deliver networks will be required. This thesis presents a method for measuring dynamic currents in power networks by measuring the magnetic fields created by these currents. The location chosen to demonstrate the technique was the supply connection between a modern ball grid array package and the underlying printed circuit board. The method, however, is general and could be applied in other locations. In Chapter 2, we will take a detailed look at the difficulties involved in the design of power delivery systems and the origins of these difficulties. The utility of current measurement will be discussed, and the basic measurement technique introduced. Chapter 3 then presents a design analysis, showing the method is feasible. We analyze the magnetic field behavior, develop the basic design equations, and estimate the measurement limits. Then in Chapter 4, we present the results of exploratory measurements made to test the method. The results show that the method is viable: measurement bandwidths of 2 GHz can be achieved, with measurement inaccuracies of approximately ten percent. Following this, in Chapter 5, we demonstrate the application of the technique to a real-world problem. We measure the dynamic supply currents for a CAM memory and discuss the implications of these data for power system design. Finally, Chapter 6 we will discuss the possibilities for the further development of the technique.

Chapter 2

Background

While continued technology scaling has been good for chip performance, it has also made formerly simple tasks, like supplying power to these chips, much more difficult. This chapter will look at the problem of engineering a power supply system for modern integrated circuits. Section 2.1 first provides an overview of the components that are involved in delivering power to the chip and explains how they are configured. Having described the power delivery system, Section 2.2 describes the requirements on this system, and the simulation tools that are used to try to ensure the integrity of power networks. Since simulation tools need to be validated by measurements, Section 2.3 then describes different techniques for measuring the quality of the voltages in the power system, including methods that measure the end points on-silicon, which matter the most. In situations where the voltages in the system do not match simulations, or show poor behavior, it is often useful to measure where the current is flowing in the system, especially in the section from the PCB through the package. It is the measurement of this current that has been difficult in the past, and Section 2.4 describes how a simple inductive loop can be used to provide essential information for debugging power supply problems.

2.1 The Power Delivery System

To begin, let's look at the components of a typical power supply for an integrated circuit (IC). Figure 2.1 shows an IC mounted on a printed circuit board (PCB), and an accompanying simple electrical circuit model. As the circuits on the IC die function, they draw both AC and DC current from VDD and return it to VSS. These currents

then pass into the on-die power distribution networks, then through the IC package and into the distribution networks in the PCB, eventually reaching the power supply. At each stage of this journey, fluctuations in the VDD to VSS voltage can occur. The on-die VDD and VSS networks are characterized by significant resistance, owing to their small dimensions. The resulting IR drop creates supply voltage changes for both AC and DC supply currents, and managing this drop is a major challenge for IC designers. In contrast, inductance is the main characteristic of IC package voltage distribution nets. This inductance originates from the fact that the VDD and VSS networks are physically separated and the VDD/VSS current loop thus encloses a non-zero area. The resulting inductance creates supply voltage changes which can be large for rapid changes in supply current. Minimizing this inductance is one of the major objectives of good package design. In modern high-performance printed circuit boards, the power networks are usually copper planes and are thus distributed LC transmission line structures. Voltage drops along these structures are created by the chip's AC supply currents. To reduce the magnitude of these voltage drops, so called "bypass" capacitors are placed across the VDD/VSS networks. These capacitors source charge to the VDD network when the IC demands more current. This reduces the rate at which current in the PCB network must change, and so reduces voltage fluctuation. Unfortunately, these capacitors themselves contain series inductance and resistance, which limits their response. Nonetheless, they are an essential part of a well designed power system, and are most effective when placed near IC packages. Bypass capacitance can also be placed across the VDD/VSS networks on silicon to perform a similar charge supply function. Addition of this on-die capacitance is often required in high performance digital integrated circuits.

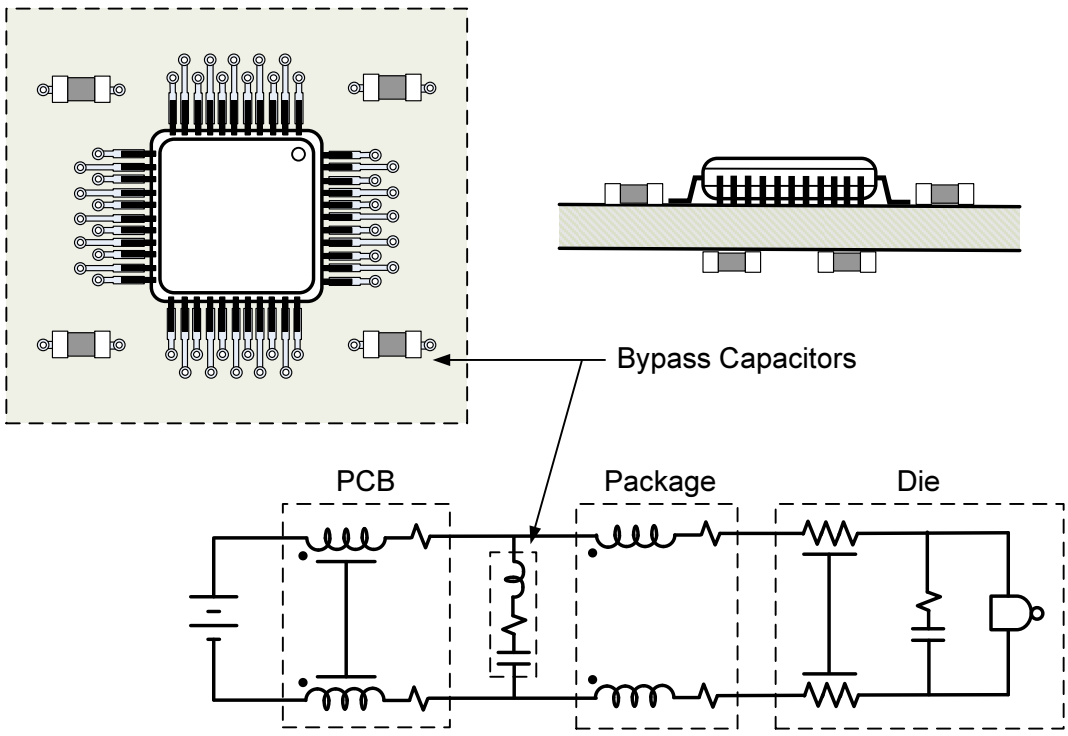


Figure 2.1 – Typical Power Supply Network

From the foregoing discussion, it's clear that power network impedances, particularly on-die resistance and package inductance, must be reduced to limit power supply voltage noise. The extent of the required reduction is determined by the magnitude of the supply current and its time rate of change, and it is here that MOS device scaling has had a major impact. Channel lengths have been reduced by more than a factor of ten over the last decade, and power supply voltages have fallen from a once ubiquitous 3.3V to values as low as 1V. Power density has increased only moderately, but the increased circuit density made possible by scaling has encouraged circuit designers to increase the number of circuits on a die. As a result, power dissipation per die has remained constant or in many cases increased. The combination has produced very large supply currents and time rates of current change. Figure 2.2 shows the feature size, supply voltage and power dissipation trends for high performance processors over the last 25 years [HAP05]. Power dissipations of 100W or more are now common, with supply voltages of around 1.2V. This corresponds to a total DC supply current of 80A or more. Even in the more moderate realm of

application specific circuits (ASICs) supply currents of 40A or more are not uncommon for large, high performance ASICs, and values of $\partial I/\partial t$ on the order of 1×10^{8} A/sec have been estimated for some designs.

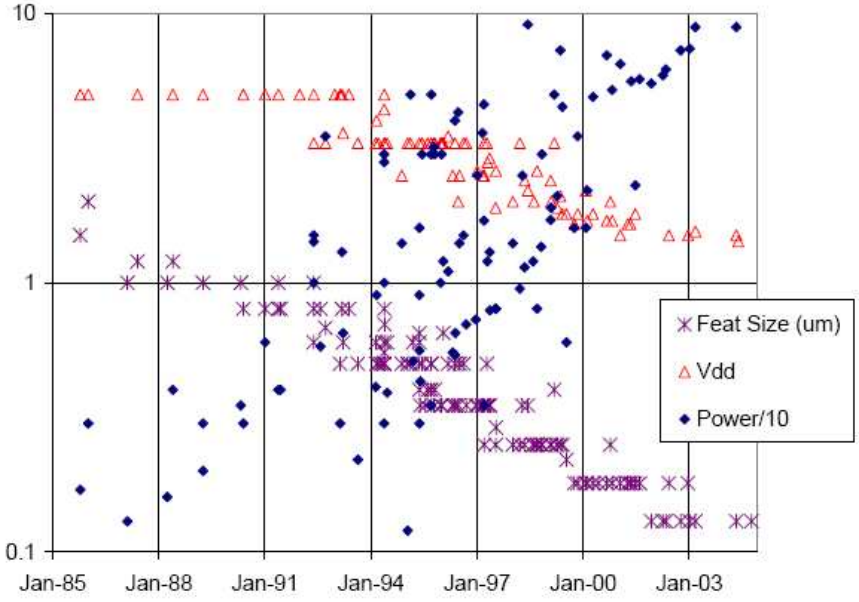


Figure 2.2 – Supply Voltage and Current Trends of High Performance Processors

The advent of such large currents and the resulting need to reduce package inductances has driven an evolution in IC package design. Figure 2.3 shows the progression of this process. The traditional plastic quad flat-pack package (PQFP), once an industry standard, has formed pins around the perimeter of the package for PCB attachment. The pins connect to a lead frame inside the package which carries power and signals inward to the edge of the die. Small bond wires connect the ends of the lead frame to pads around the perimeter of the die. On-die metal layers then distribute power across the die area. Since the VDD and VSS leads are carried from the package perimeter in to the die edge, the VDD/VSS current loops enclose large areas, and large inductances are the result. The opportunities to reduce these inductances are limited: more VDD/VSS pins can be used, at the expense of signal pins, and/or a finer lead pitch can be used, subject to the limits of PCB assembly technology. Furthermore, the bond wire attachment around the perimeter of the die

results in long power routes in on-die metal layer and hence significant resistance. The development of the ball grid array (BGA) package and the direct die attachment process mitigates both of these problems. In a BGA package, PCB attachments in the form of small solder balls are uniformly distributed across the area of the package bottom. This allows a large block of VDD and VSS balls, usually alternating in both *x* and *y* dimensions, to be place directly under the die. These balls then connect to VDD and VSS planes in the package. The direct die attachment process then places and array of pads across the die area. Small bumps of solder then attach the die directly to the top of the BGA package. The VDD/VSS current loop areas, and thus inductances, are minimized, and the distribution of VDD and VSS pads across the area of the die minimizes the routed length of on-die power nets and hence their resistance. Finally, the BGA package makes it possible to mount bypass capacitors directly on the top surface of the package substrate near the die.

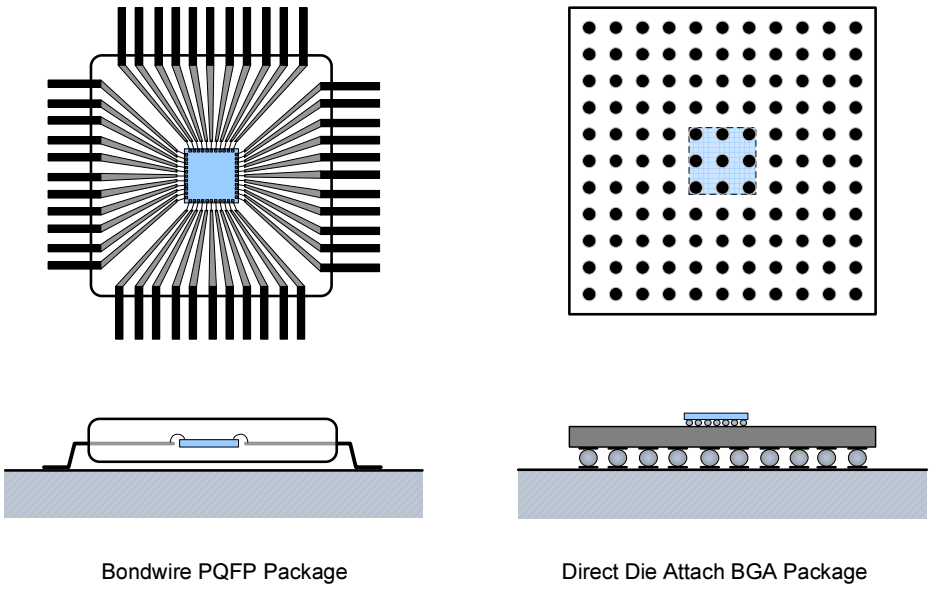


Figure 2.3 – IC Package Evolution

As IC packaging technology has evolved, so too have high performance printed circuit boards. Figure 2.4 shows a cross-section through a modern PCB under a BGA package. Routed power networks have been replaced with solid copper power and

ground planes, and for high current supplies, these planes are placed immediately adjacent to each other with no intervening signal traces. This minimizes the VDD/VSS current loop area and resulting inductance, and lowers the impedance of the power/ground network. To accommodate BGA packages, an array of vias are placed under the BGA to connect the package balls to the PCB power/ground planes and to signal traces. PCB bypass capacitors are most effective when placed near the source of charge consumption [AWC03]. Since the core power balls are located in a block centered under the die, bypass capacitors are often placed on the back side of the board, directly behind the BGA and are connected across the VDD/VSS vias. Again, this minimizes current loop area and thus the series inductance between the capacitance and the package balls. The resulting VDD and VSS currents are also shown in Figure 2.4. VDD current flows into a VDD via from the VDD plane and from any bypass capacitor on the backside of the PCB. The sum of these currents then passes into the BGA package ball. Similarly, the VSS current from a package ball passes into the VDD via, and thence flows into the VSS plane and any bypass capacitor attached to the via.

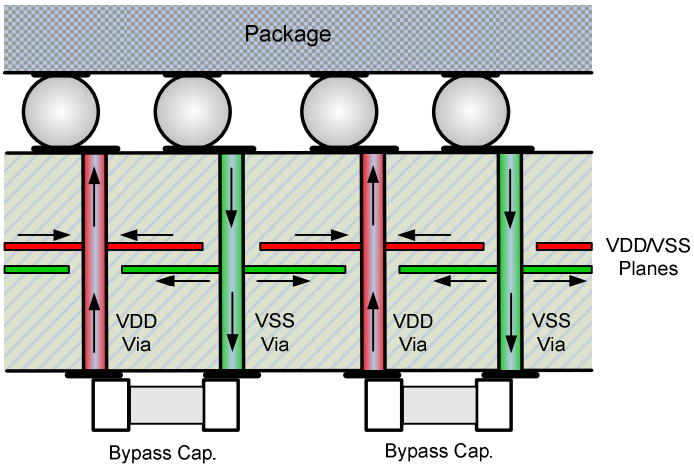


Figure 2.4 – PCB Cross-section under BGA Package

For AC power currents with frequencies above 14 megahertz, a VDD/VSS plane pair forms a parallel plate waveguide structure. The currents are carried on the plane surfaces facing each other, and the waveguide completely contains the resulting

electric and magnetic fields. While the VDD/VSS plane pair can be located anywhere in the thickness of the PCB, the pair supplying power for IC core logic is often located near the center because designers feel that this strikes a balance between plane to package inductances and bypass capacitor to plane inductances. The planes and bypass capacitors together form a complex electrical system which can have numerous resonant modes. These modes can drastically increase supply network impedance and increase supply noise, so steps must be taken to limit their effects. The distribution of bypass capacitors of appropriate values across the PCB can help [SAF99], and using lossy capacitors can also be beneficial [ZH02]. The use of high dielectric constant layers between the VDD/VSS plane pair to form a distributed bypass capacitor is also under development, and can be very beneficial [MHC03]. The use of ferro-magnetic coatings on the plane surfaces has also been studied as a way to lower the Q factor of power system resonances [WT05].

2.2 The Importance of Power Integrity

From our review of power distribution it's clear that distributing large supply currents with high voltage quality can be difficult and potentially expensive. The important questions are what level of voltage quality is required and what design methods can be used to estimate the voltage quality that can be expected from a given design. In addressing the question of voltage quality, we must first understand the effects of supply voltage variation on CMOS circuits. In digital circuits, extreme fluctuations in supply voltage can cause malfunctions, but owing to the nonlinear nature of their operation, most digital circuits can tolerate relatively large variations in power supply voltage and still function correctly. The largest impact of supply noise is variation in gate delay times, which results in reduced system performance. The source of this variation can be understood using the simple circuit shown in Figure 2.5. Here a CMOS inverter drives another CMOS inverter. Assuming the two inverters are not connected by a long metal route, the load on the driving inverter is essentially a capacitance, C_L, composed of the drain to bulk parasitic capacitances of the driving transistors Q_P and Q_N and the input capacitance of the driven inverter. The driver

output voltage, V_O, rises when C_L is charged from VDD through the effective output resistance of Q_P and falls when C_L is discharged to ground through the effective output resistance of Q_N.

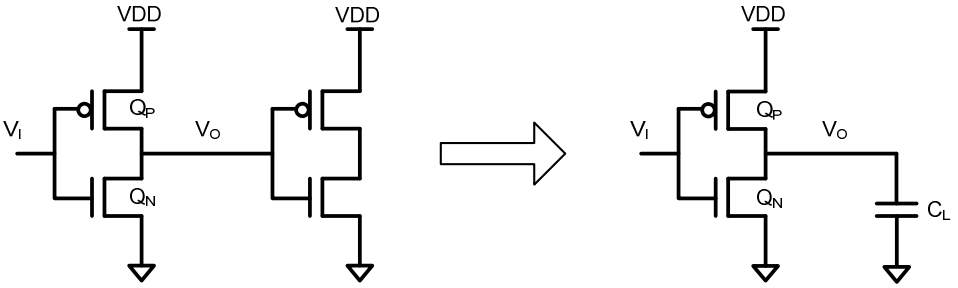


Figure 2.5 – CMOS Inverters

In well designed CMOS gates, the input switching threshold is very close to VDD/2 and changes minimally with variation of VDD. Thus the delay time of the driving inverter in Figure 2.5 can be taken as the time required for V_O to rise (or fall) to VDD/2. Exact calculations for this time are quite complex (see for example [Hor83]), but a simple first order approximation is adequate for our purposes. We assume that the driving MOS transistor and the load capacitance form a simple RC circuit and therefore that voltage V_O will rise (or fall) exponentially with time. So the low-to-high and high-to-low delay times are $t_{pLH} = \ln(2)R_{OP}C_L$ and $t_{pHL} = \ln(2)R_{ON}C_L$, respectively. In a well designed gate, these times will be roughly equal. To estimate the effect of supply noise, we need to understand how R_{OP} and R_{ON} change with VDD. Since modern short channel MOS transistors operate in velocity saturation for all but the lowest values of V_{DS}, we can use the approximation that $R_{ON} = R_{OP} = VDD/I_{DSAT}$ where I_{DSAT} is given by ([SKM84], [TKM88]):

$$I_{DSAT} = W_{mos} C_{ox} v_{SAT} \frac{(V_{DD} - V_T)^2}{(V_{DD} - V_T) + E_C \ell} \qquad (2.1)$$

The saturation velocity, critical electric field value, and unit area gate capacitance (v_{SAT}, E_{SAT}, C_{ox}) depend on the silicon process node, and the channel width and length

(W_{mos}, ℓ) depend on transistor geometry. Combining this with the expressions for delay then gives the result:

$$t_{pLH} = t_{pHL} = \ln(2)\left(\frac{C_L}{W_{mos} C_{ox} v_{SAT}}\right)\left[1 + \frac{E_C \ell}{V_{DD} - V_T}\right]\frac{V_{DD}}{V_{DD} - V_T} \qquad (2.2)$$

Since the transistors are assumed to be heavily velocity saturated, the term in the square brackets is near unity, and so delay scales as $V_{DD}/(V_{DD} - V_T)$. Other approximations for I_{DSAT} can be used ([TN98], [GM01]) and empirical expressions for R_O have been proposed [Wor89], but all show that delay depends on supply voltage. Because of this, supply noise creates uncertainty in propagation times which can require the insertion of extra delays and reductions in clock frequencies in order to close timing in digital systems, at the cost of reduced performance. To achieve high performance, supply voltage tolerances have often been tightened to ±5% of nominal. With supply voltages hovering around 1 volt, this translates into a variation of ±50 mV. For analog circuits the constraints can be even tighter. Supply voltage noise in analog circuits can cause numerous problems such as spurious spectral components in oscillators, and jitter in phase locked loops and clock recovery circuits. A noise limit of 25 mV peak-to-peak on analog supply rails is not uncommon. Meeting such a requirement can be difficult when such circuits are used in mixed-signal chips containing both digital and analog circuits.

With such tight constraints on supply voltage, extensive use of numerical simulation tools is now essential to the design of power networks that perform adequately and are cost effective. The nature of the problem, however, poses challenges to these tools. Transient currents in the supply networks of digital integrated circuits are produced by the activity of CMOS circuits that are highly non-linear in nature. On the other hand, the interconnect portion of the supply network is a large, linear system containing both lumped and distributed circuits. Thus we are faced with a dilemma. The non-linear circuits must be simulated in the time domain with tools such as Spice, whereas the interconnect portion is most efficiently simulated either in the time domain using a fast linear solver or in the frequency domain. Using

Spice to simulate the entire power system produces untenably long simulation times. Furthermore, the supply interconnect is a large system that often cannot be sectioned into smaller pieces without significant loss of simulation accuracy. This is particularly true of on-die power grids and ball grid array packages. As a result, the sheer size of the resulting problem can overwhelm many simulation tools.

To make power system simulation a tractable problem, it is usually necessary to introduce simplifications to reduce the problem size. One such simplification is to divide the problem into two simulations [BPC01]. The CMOS circuit operation is simulated with a constant supply voltage using Spice, and the resulting supply currents applied to the interconnect model, which is simulated using a fast linear simulator. The resulting voltage fluctuations at the circuit level are then used to determine the effects on performance. Another approach is to instantiate a small number of CMOS circuits as pilots and replicate identical neighboring circuits as current sources controlled by the pilot circuits. The circuits and interconnect are then simulated together. This technique can be particularly useful in simulating the supply voltage noise generated by large blocks of simultaneously switching output circuits. Simplifications are also often required in dealing with the interconnect model, since the full interconnect model may be so large that simulation time is too long even with the use a fast linear solver. To further reduce simulation time, model order reduction can be employed. The transfer function of a complicated model will contain many higher order terms that do not contribute materially to the response of the model to the applied stimulus. Model order reduction attempts to simplify the model by eliminating these terms while leaving the relevant terms intact. What is relevant will depend on the spectrum of the stimulus and the degree of accuracy required.

Necessary as they are, these simplifications bring with them the possibility of appreciable inaccuracy in the predicted voltage supply noise at the circuit level. Partitioning the problem into separate non-linear and linear simulations introduces error. Iteration reduces the error, but the iteration may diverge. Simulation using pilot circuits controlling blocks of current sources will give erroneous results if the block size is too large. Finally, model order reduction can give good results but can also

produce models that are unstable and/or non-casual. Unstable models are fairly easily detected as they produce wild oscillations in the results as simulation proceeds. Non-causality is a far more insidious problem. Non-causal models exhibit output response behavior that is not the result of the input stimulus. The effect is often subtle and difficult to detect, but leads to considerable errors in simulation results. Some modeling tools (e.g. Broadband Spice from Sigrity Inc., ADS from Agilent Inc.) now attempt to enforce both stability and causality in the models they produce. To do so, they make (hopefully) small changes to the transfer function to ensure that the resulting model is stable and causal.

2.3 Voltage Measurement Methods

With many possible sources of error, it is clearly desirable to validate simulation and modeling methods by comparing the simulated supply voltage behavior at critical points in the power system to the corresponding values measured in real systems. These measurements have traditionally been made at the V_{DD} and V_{SS} pins of the integrated circuit package(s) using an oscilloscope. When die sizes were small (≤ 4 mm^2) and operating frequencies low (≤ 50 MHz), such measurements were perfectly adequate. The continued advancement of CMOS technology has produced large die operating at frequencies into the GHz range. As operating frequencies increased and the noise spectrum widened, the distance between measurement point and ground reference had to be decreased to reduce the loop area subject to stray noise reception. The allowable distance today can be as small as a few millimeters. At the same time, these larger die require much larger packages, and, as we have seen, the die/package/PCB combination forms a complicated system whose internal behavior is not readily observable from voltage measurements across the package pins. Certainly, supply voltage fluctuations at the printed circuit board level must stay within prescribed limits, and measurements on the PCB are required to verify this. But on-die measurements of supply voltage are now required to verify power system integrity at the circuit level and validate simulation results.

Several schemes have been advanced to make on-die supply voltage measurements. One of the simplest is the method used by Darnauer et al. [DCS99]. In this approach, matching 400Ω PMOS resistors connect adjacent locations on the VDD and VSS networks to signal tracks routed out to two package pins. Differential measurement across these pins gives the time varying supply voltage at the monitoring point. Using this method, the authors investigated the affects of bypass capacitor placement and package technology on supply voltage noise. On-die measurements have also been made. Muhtaroglu et al. [MTR04] demonstrated measurement circuits that can detect supply voltage overshoots and undershoots that exceed programmable limits over an adjustable time window. Using a number of these circuits linked by a scan chain, the authors collected voltage noise magnitude and time distribution data for a large microprocessor die. Petrescu et al. [PPV06] have proposed a family of measurement circuits, including a voltage measurement circuit that uses a seven bit DAC controlled via a scan chain and a fast synchronous comparator to measure supply voltage level and droop. On-die sub-sampling oscilloscope heads for supply voltage measurement have been demonstrated by both Takamiya et al. [TMN02] and Inagaki et al. [IDT06]. Inagaki obtained good agreement between simulation and measurement of supply noise on a test chip. An interesting approach has been demonstrated by Alon et al. [ASH05]. In this scheme, dual samplers and simple, VCO based AD converters are used to extract the autocorrelation function of the supply voltage noise. From this, the power spectral density of the noise is obtained as the Fourier transform of the autocorrelation function. All of these schemes, particularly those using on-die samplers, can provide valuable measurement data for validating the performance of power distribution networks and the quality of the supply voltage at the circuit level.

2.4 Proposed Current Measurement Method

Voltage measurements tell us much about the integrity of a supply network. Our understanding can, however, be extended if we have knowledge of the transient currents in the supply networks. It is the passage of these currents through the non-zero impedances of the power networks that generates the supply voltage noise. If

measured supply voltage noise differs significantly from the predictions of simulation, a likely cause is an erroneous impedance calculation. Knowledge of the actual network impedances can help to locate the errors. Absent measured transient current data, methods to date for determining supply network impedance under operating conditions have relied on various means of estimating currents from voltage measurements ([KHR04], [WCH03], [WLS04]). The difficulties and potential inaccuracies of these methods can be eliminated if fine-grained measurements of transient currents can be made. By measuring the transient currents in the V_{DD}/V_{SS} pins of an integrated circuit package and combining these data with on-die voltage measurements, the transfer impedances between the pins and the die could be directly obtained. These results could then be compared to the values predicted by simulation. Also, package pin current measurements would allow system designers to access the effectiveness of PCB bypass capacitance when lack of information about chip internals prevents simulation.

These current measurements require a current sensor of small physical size that has a wide measurement bandwidth, ideally 1 GHz or more. With such a wide bandwidth, the sensor should also have low internal noise so that an adequate signal to noise ratio (SNR) can be achieved. Furthermore, measurements should have minimal impact on the measured circuit. All of these requirements argue for the use of a single turn inductive loop as a sensor. Such sensors have been proposed for IDDT testing ([NIA04], [ABS05]). The basic idea behind the approach is simple. A current carrying conductor generates a surrounding magnetic field. If a small, single turn loop is placed in this magnetic field, changes in the conductor's current will induce a voltage across the loop, and from this voltage, the AC current can be found. These loops can be made very small, and so have low self inductance. This gives a high upper measurement frequency. Furthermore, they are a metal resistor with a few milliohms of resistance, so they have no flicker or shot noise and only a small amount of thermal noise. Effectively, the noise floor is set by the voltage measurement instrumentation. Finally, since the induced voltage grows linearly with frequency while the random noise in the

instrumentation grows as the square root of frequency, SNR does not degrade with increases in measurement bandwidth.

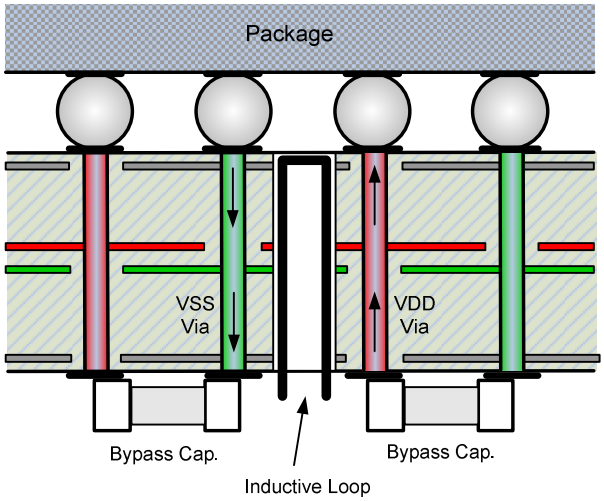


Figure 2.6 – Inductive Loop Location

There are, of course, penalties associated with induction loops. They cannot measure DC fields, and so DC currents cannot be measured. Since we are interested primarily in high frequency transient currents, the lack of a DC reading is tolerable. Induction loops also have a large magnetic aperture. The result, in this application, is that currents from multiple adjacent package pins will contribute to the voltage induced in the loop. For verification of simulation results, this effect can be predicted and thus presents no fundamental problems. For stand alone current measurements, measurements at multiple locations can be made, which allows removal of this magnetic crosstalk. Figure 2.6 shows how an induction loop can be inserted in a printed circuit board to measure core VDD/VSS via currents. A non-plated hole is placed midway between a VDD and VSS via pair. A small loop is then inserted into this hole with the loop plane lying in the plane containing the vias. The VDD and VSS currents are in opposing directions and so create circular magnetic fields threading the loop in the same direction. This increases the magnitude of the induced loop voltage. Finally, note that all of the VDD/VSS BGA ball currents are carried through that portion of the vias between the VDD/VSS plane pair and the package. The section of

the vias below the planes will carry current if there are bypass capacitors attached to the via ends on the backside of the PCB. This current can be measured by inserting the loop only up to the planes and taking measurements. This value can then be subtracted from the reading with the loop fully inserted to recover the BGA ball currents.

Chapter 3

Design Analysis

Using a single turn inductive loop to measure via currents depends completely on the magnetic fields surrounding the vias and on the response of an induction loop to these fields. This chapter develops the understanding necessary to implement a practical sensor. Section 3.1 deals with the magnetic field surrounding the vias, while Section 3.2 considers the behavior of the induction loop sensor. Section 3.3 then explores the measurement limits of this design. Both upper and lower frequency limits are considered. Finally, Section 3.4 looks at the effect of probing on the measured circuit.

3.1 The Magnetic Field Surrounding PCB Vias

The proposed measurement approach relies on the fact that a current carrying conductor is surrounded by a magnetic field, and the intensity of this field is proportional to the magnitude of the current. If a small, single turn loop is placed in this field, changes in the conductor's current will induce a voltage across the loop given by Faraday's Law: $V_{loop} = \frac{\partial}{\partial t} \iint \vec{\mathbf{B}} \bullet d\vec{\mathbf{A}}$. To make practical use of this principle, however, we must know the spatial distribution of the magnetic field. This can be done with a straightforward application of Maxwell's equations to the via/PCB configuration of Figure 3.1. As shown, high performance printed circuit boards have ground (or power) planes as their next to outermost layers to reduce electromagnetic radiation from the board. Thus between the VDD/VSS plane pair supplying the vias we want to measure and each outer surface there is at least one (possibly several) solid

plane(s). The skin depth, δ_S, of AC electric and magnetic fields in these layers is given by [RWV67]:

$$\delta_S = \sqrt{\frac{\rho}{\pi f \mu}}$$

where ρ = 17.2 nΩ-m for copper, f is the field frequency, and $\mu = \mu_o = 4\pi \times 10^{-7}$ H/m for the materials used in printed circuit boards. Typical printed circuit board planes are 18 μm thick copper. Setting δ_S = 18 μm and solving for f gives $f \cong 14$ MHz. Thus over most of the frequency range of interest it will be the case that δ_S is much less than the thickness of the PCB metal layers, and we can approximate the pairs of planes as perfect conductors which completely contain electric and magnetic fields between them.

To predict the magnetic field produced by a via's current we proceed as follows. Figure 3.1 shows a single current carrying via passing through a plane pair. Since the skin depth is much less than the thicknesses of the planes, we assume that the conductivity of the planes approaches infinity.

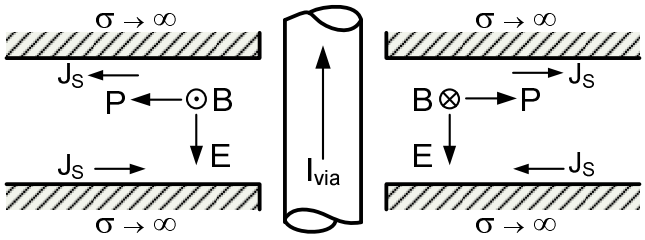


Figure 3.1 – Cross Section of Via and Plane Pair in Region A

The governing equations are Maxwell's equations, repeated here for reference (SI units):

$$\vec{\nabla} \bullet \vec{\mathbf{E}} = \rho \qquad \vec{\nabla} \times \vec{\mathbf{E}} = -\frac{\partial \vec{\mathbf{B}}}{\partial t}$$

$$\vec{\nabla} \bullet \vec{\mathbf{B}} = 0 \qquad \vec{\nabla} \times \vec{\mathbf{B}} = \mu \vec{\mathbf{J}} + \mu \varepsilon \frac{\partial \vec{\mathbf{E}}}{\partial t}$$

Inside the metal planes, $|\vec{\mathbf{E}}|$ = 0 and so: $\partial\vec{\mathbf{B}}/\partial t = 0$. Thus there is no alternating magnetic field inside the metal. The curl equations require that $\vec{\mathbf{E}}$ and $\vec{\mathbf{B}}$ are at right angles. Since, $\vec{\mathbf{E}}$ parallel to the plane surface must be zero, $\vec{\mathbf{B}}$ perpendicular to the surface must also be zero, and the $\vec{\mathbf{B}}$ field just outside the plane is parallel to the surfaces. Hence there is a curl in the $\vec{\mathbf{B}}$ field, and the direction of this curl is along the surfaces of the planes. This then requires that there be a current, $\vec{\mathbf{J}}_{\mathbf{S}}$, along the surfaces of the planes. In the space between the planes, $|\vec{\mathbf{J}}|$ = 0, and the electric and magnetic fields are at right angles to each other. From symmetry and the requirement that $\nabla \bullet \vec{\mathbf{B}} = 0$, the $\vec{\mathbf{B}}$ field is circular with the center located on the axis of the via. Thus the $\vec{\mathbf{E}}$ field is perpendicular to the plane surfaces, and the surface currents, $\vec{\mathbf{J}}_{\mathbf{S}}$, flow along radii from the via axis. The result is a plane wave confined by the plane pair and propagating radially out from the via. Figure 3.1 shows the electric and magnetic field vectors of the wave along with the Poynting vector, $\vec{\mathbf{P}}$. The dimensions of interest, however, are on the order of a few centimeters, much smaller than the wavelengths of the target signals. A 1 GHz signal has a wavelength of 15 cm in the FR4 dielectric typically used in printed circuit boards. We will therefore invoke the quasi-static approximation. Ampere's Law then reduces to the magneto-static form $\vec{\nabla} \times \vec{\mathbf{B}} = \mu \vec{\mathbf{J}}$. This then gives: $B = \mu I_{via} / (2\pi r)$.

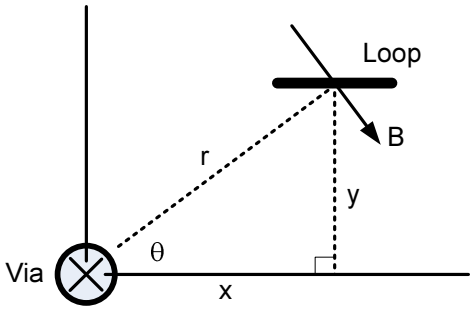


Figure 3.2 – Top View of Via and Induction Loop

To calculate the loop response we first assume that the current densities in all power and ground planes are equal in the vicinity of the loop, and therefore, power/ground pairs induce no signal in the loop. The induced voltage as a function of loop location is then easy to calculate. Figure 3.2 shows a top view of a current carrying via and an induction loop with its center located at a distance *r* from the via center and rotated through an angle θ. The loop has a width *W* in the x direction and height *h* parallel to the via's axis. The voltage, V_{out}, induced in a loop is derived using Faraday's Law of Induction with the magnetic field intensity given by $B = \mu_0 I_{via}/(2\pi r)$. Since either of the two loop terminals can be defined as the positive terminal, we will choose the definition that eliminates the minus sign from Faraday's Law.

Then:

$$\begin{aligned} V_{out} &= \frac{\partial}{\partial t}\iint \vec{\mathbf{B}} \bullet d\vec{\mathbf{A}} = \frac{\partial}{\partial t} h \int_{u=x-W/2}^{u=x+W/2} (B\cos\theta)\, du \\ &= \frac{\partial I_{via}}{\partial t} h \frac{\mu_o}{2\pi} \int_{u=x-W/2}^{u=x+W/2} \frac{u}{u^2 + y^2}\, du \\ &= h\frac{\mu_o}{4\pi} \ln\left\{ \frac{\left(x+\frac{W}{2}\right)^2 + y^2}{\left(x-\frac{W}{2}\right)^2 + y^2} \right\} \frac{\partial I_{via}}{\partial t} \end{aligned} \tag{3.1}$$

Hence the mutual inductance, as a function of *x* and *y*, is:

$$M(x,y) = h\frac{\mu_o}{4\pi} \ln\left\{ \frac{\left(x+\frac{W}{2}\right)^2 + y^2}{\left(x-\frac{W}{2}\right)^2 + y^2} \right\} \tag{3.2}$$

Since ferromagnetic materials are rarely used in printed circuit boards, the system is linear, and we can superpose the loop voltages created by individual vias to obtain the total loop voltage.

3.2 Sensor Design

With the induced loop voltage function known, the question is what the loop dimensions should be. Figure 3.3 shows an induction loop positioned midway between a VDD/VSS via pair. The loop has a width of *W* along the *x* axis and *h* along the axes of the vias. The center to center via pitch is *D*. The VDD and VSS current magnitudes are equal, and the currents are in opposite directions.

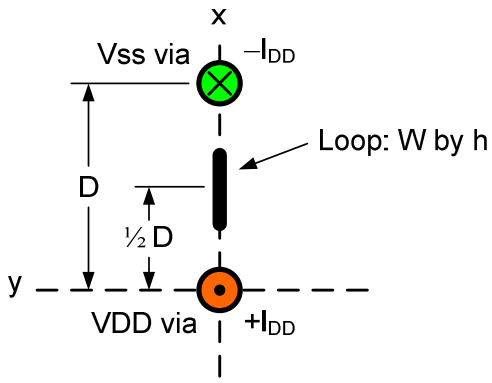


Figure 3.3 – Loop and Via Pair

The loop center coordinates are (D/2, 0). Using these values of *x* and *y*, equation (3.1) can be rewritten as:

$$\frac{V_{out}}{V^*} = 2\ln\left(\frac{\delta+1}{\delta-1}\right)^2 \qquad (3.3)$$

where $V^* = h\frac{\mu_o}{4\pi}\frac{\partial I}{\partial t}$ and $\delta = \frac{D}{W}$

This ratio can be considered a geometrical gain factor and its value is plotted against δ in Figure 3.4.

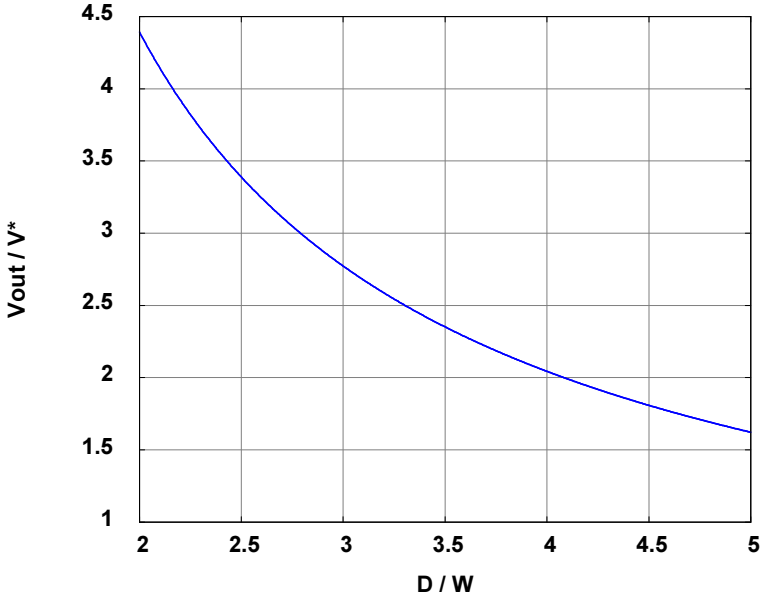


Figure 3.4 – Geometrical Gain Factor

This plot would imply that the loop width, W, should be made as large as possible. PCB manufacturing tolerances, however, make it impossible to perfectly position the loop. To assess the effects of loop misalignment, we can rewrite equation (3.1) in terms of displacement from the ideal position of ($D/2$, 0). This gives:

$$\frac{V_{loop}}{V^*} = \ln\left(\frac{(\delta+2\chi+1)^2+(2\psi)^2}{(\delta+2\chi-1)^2+(2\psi)^2}\right) + \ln\left(\frac{(\delta-2\chi+1)^2+(2\psi)^2}{(\delta-2\chi-1)^2+(2\psi)^2}\right) \qquad (3.4)$$

where $\chi = \frac{x}{W}$ and $\psi = \frac{y}{W}$

Here, δ and V^* have the same definitions as in equation (3.3), and x and y are the displacements from ($D/2$, 0). Equation (3.4) is plotted against χ in Figure 3.5 and against ψ in Figure 3.6 for δ = 2, 3, 4 and 5. The plots show that a value of δ = 4, corresponding to a loop width of $W = D/4$, is a reasonable design compromise. The output voltage of a loop this size changes by less than 10% of its centered value for x or y displacements of half a loop width, and the geometric gain factor has a reasonable value of 2.04.

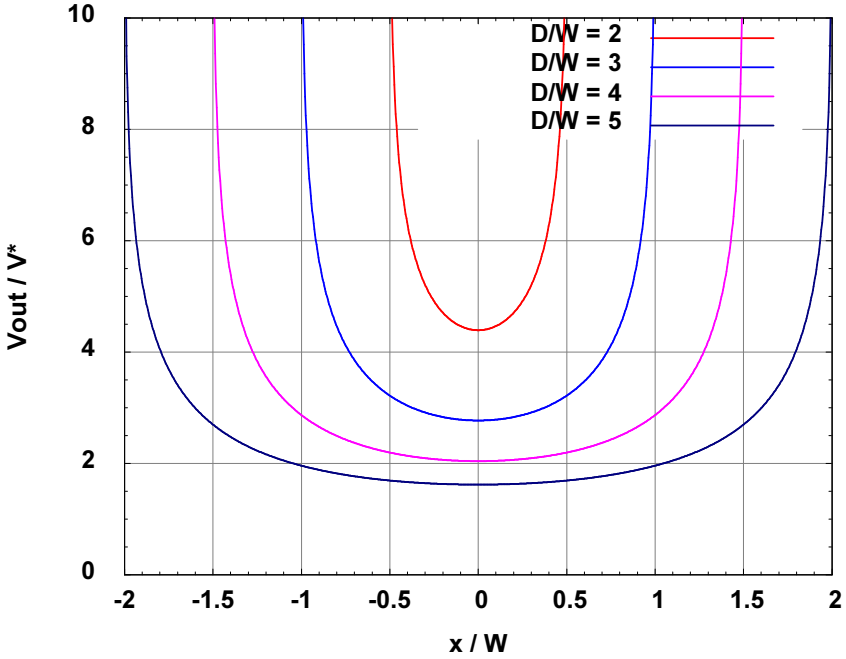


Figure 3.5 – Effect of Misalignment in ***x***

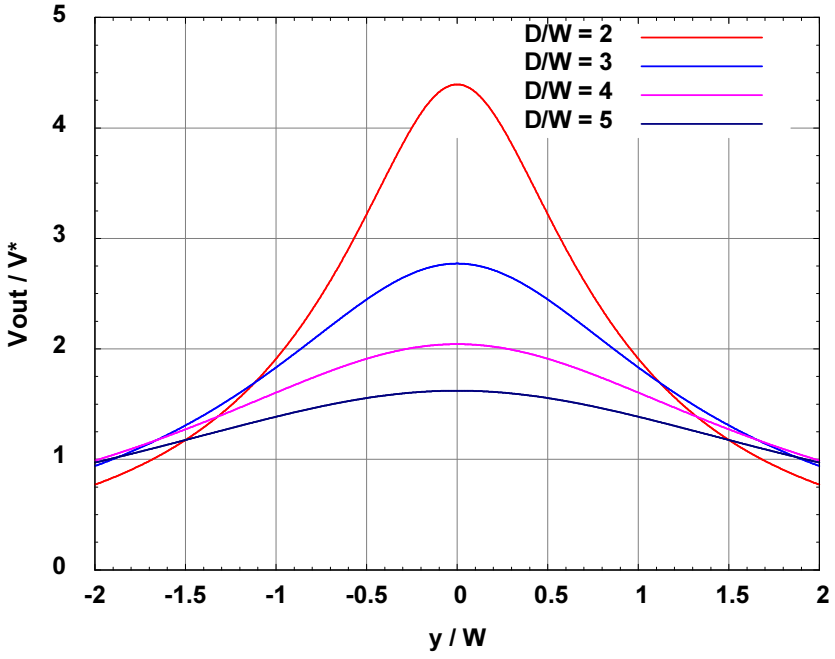


Figure 3.6 – Effect of Misalignment in *y*

To build the loop, we can use standard PCB technology, and employ a 76 μm (3 mils) wide copper trace on a 100 μm (4 mils) thick FR4 substrate to form the loop. The most commonly used BGA ball pitch is 1 mm, so the active loop width should be 250 μm (10 mils). The overall width is 100 + 2 × 76 = 402 μm (16 mils). Happily, a 500 μm (20 mils) diameter non-plated hole can be reliably drilled between vias on a 1 mm pitch, so this loop can be inserted into printed circuit boards.

3.3 Measurement Limits

Constructing a loop appears feasible, so next we need to address the question of measurement limits. This is really two questions: what is the minimum detectable signal and what is the overall measurement bandwidth. Let's first look at the question of minimum detectable signal. The loop itself is nothing more than a metal film resistor. A 3 mm long (i.e. h = 3 mm) loop of 76 μm wide, half ounce (18 μm) thick copper trace enclosing an air gap of 250 μm has a resistance of less than 1 mΩ. So the loop generates no shot or flicker noise and only a miniscule amount of thermal noise. The overall noise floor is thus set by the measurement instrument(s) used. A commonly used instrument is a high performance real time sampling oscilloscope, such as the Tektronix TDS7704B. This unit has a sampling rate of 20 Gs/sec and a front side bandwidth of 7 GHz. Its equivalent noise voltage is roughly 1 nV/$\sqrt{Hz}$, and assuming a first order roll-off, this gives a total equivalent noise voltage of 105 μV. Using a signal to noise ratio (SNR) of 1 as the detection limit, the minimum detectable signal level is 105 μVrms. The sensitivity of the loop will depend on the effective loop height, h. This will depend on the exact board thickness and VDD/VSS plane pair location, but high performance PCB thicknesses are in the 2.5 mm to 3 mm range. With h = 3 mm, equation (3.3) gives a mutual inductance of M = 613 pH. For a sinusoidal VDD/VSS via current $\partial I/\partial t = 2\pi I_0 f$ where f is the sinusoid's frequency, and I_o is its amplitude. Therefore, the root mean square signal voltage is $V_s = 2\pi M I_0 f/\sqrt{2}$. Arbitrarily setting I_o = 10 mA, the minimum required frequency is 3.9 MHz. The corresponding required peak $\partial I/\partial t$ is 0.25 mA/ns. We can then

normalize this to give a minimum $\partial I/\partial t$ requirement of 0.75 mA/ns/mm of via pair length. Finally, note that for measuring repetitive events, we can average a large number of samples. This improves the signal to noise ratio by $\sqrt{N}$, where N is the number of samples averaged, and lowers the minimum required $\partial I/\partial t$.

Now let's take up the question of measurement bandwidth. This is largely a question of identifying the upper measurement frequency. The loop will be connected to the input of a measurement instrument which has purely resistive input impedance. Figure 3.7 shows the resulting equivalent electrical circuit. The resistance, R, is the input resistance of the instrument, and the inductance, L, is the self inductance of the loop. The loop response is then determined as follows.

For sinusoidal excitation: $$V_i = M\frac{\partial}{\partial t} I_{via} = s\,M\,I_{via}(s)$$

The transfer function is: $$T(s) = \frac{V_o}{V_i} = \frac{1}{1+s(L/R)}$$

Therefore the transfer impedance is: $$\frac{V_o(s)}{I_{via}(s)} = M\left(\frac{s}{1+s(L/R)}\right)$$

Thus for frequencies $f < L/(2\pi R)$, the loop response is that of a differentiator. Therefore, below this frequency the loop voltage must be integrated to recover the via current. Above this frequency, the loop voltage is proportional to sensed current. While it might be possible to recover and process current data in two regimes, it is cumbersome, and the SNR will degrade because the signal amplitude is fixed above the break, while the random noise will grow as $\sqrt{f}$. Therefore, we would like the break frequency to equal or exceed our desired upper measurement frequency of 1 GHz. Current measurements can then made by integrating the induce loop voltage. This integration produces a quasi low-pass response:

$$\frac{\frac{1}{s}V_0(s)}{I_{via}(s)} = M\left(\frac{1}{1+s\frac{L}{R}}\right) \tag{3.5}$$

This is plotted in Figure 3.7. The response is only quasi low-pass because of the minimum signal requirements considered earlier; we cannot measure DC currents.

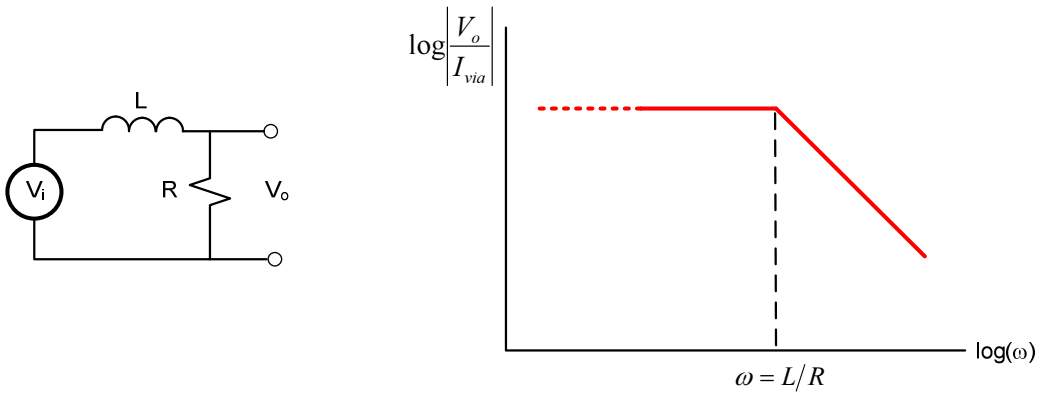


Figure 3.7 – Bandwidth of Resistively Terminated Loop with Integration

Since R = 50Ω for all high frequency measurement instruments, the bandwidth question comes down to what is the self inductance, L, of the loop. Since the loop height needs to equal or exceed the thickness of the thickest PCB we want to measure, we set h = 3 mm. Then, since the loop is very much longer than it is wide, we can treat it as two parallel conductors. The inductance can then be calculated using the formula [Gro40]:

$$L \cong 4h\left[\ln\left(\frac{d}{B+C}\right)+1.5\right] \tag{3.6}$$

where L is in nano-henries, h is the loop height in centimeters, d is the center to center spacing of the two conductors, B is the width of the conductors and C is the thickness of the conductors. Using the dimensions of our loop: h = 3 cm, d = 250 µm + 76 µm, B = 76 µm and C = 18 µm, the inductance is L = 3.2 nH. With R = 50Ω, this gives a break frequency of 2.5 GHz. which exceeds the minimum desired upper limit of 1 GHz. The loop construction approach thus seems feasible, and we can simply integrate

the loop voltage. Instruments like the Tektronix TDS7704B sampling oscilloscope can output their digitized measurement data, so this integration can be done numerically.

3.4 Effects on the Measured Circuit

Finally, we should look at what this measurement scheme does to the measured circuit. There are really two effects to be considered. The first is the effect a resistively terminated loop has on the VDD/VSS circuit impedance. The second is the effect the 500 μm non-plated hole has on the impedance of the underlying VDD/VSS plane pair. Taking these in order, we will first look at the effect the loop has on via circuit impedance. Referring Figure 3.8, we see that a VDD/VSS via pair and the loop form an air core transformer with the loop as the secondary winding and negligible series resistance. Using the sign convention shown in the figure, the voltages and currents can be described by the equations for a transformer:

$$V_1 = L_1 \frac{dI_1}{dt} + M \frac{dI_2}{dt} \qquad V_2 = M \frac{dI_1}{dt} + L_2 \frac{dI_2}{dt}$$

where L_1 is the V_{DD}/V_{SS} via circuit self inductance, L_2 is the loop self inductance and M is the mutual inductance between the via pair and the loop.

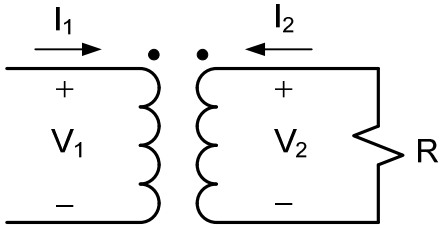


Figure 3.8 – Air-core Transformer

For steady state sinusoids these equations can be written as:

$$V_1 = j\omega L_1 I_1 + j\omega M I_2$$
$$V_2 = j\omega M I_1 + j\omega L_2 I_2$$

Noting that $V_2 = -RI_2$, we can solve for the impedance seen at the primary, giving:

$$Z_1 = \frac{V_1}{I_1} = R\left[\frac{(\omega M)^2}{R^2 + (\omega L_2)^2}\right] + j\omega\left[L_1 - L_2\frac{(\omega M)^2}{R^2 + (\omega L_2)^2}\right] \qquad (3.7)$$

Notice that resistively terminating the loop lowers the effective V_{DD}/V_{SS} circuit inductance and that the magnitude of the reduction increases with frequency. To calculate the via circuit self inductance, we treat the circuit as consisting of two circular conductors spaced a uniform distance apart. The inductance can then be calculated using the formula [Gro39]:

$$L_1 = 4l\left[\ln\left(\frac{d}{r}\right) - \frac{d}{l} + \frac{1}{4}\right] \qquad (3.8)$$

where L_1 is in nano-henries, l is the via length in cm, d is the via pitch and r is the via radius. The effects on Z_1 are greatest when L_1, L_2 and M are large, so we will here use the maximum board thickness of 3 mm. The via pitch is d = 0.1 cm, and the via radius is an industry standard 25 μm (10 mils). Equation (3.8) then gives L_1 = 2.4 nH. The mutual inductance can be calculated using equation (3.2), giving M = 613 pH, and equation (3.6) gave L_2 = 3.2 nH. Then using equation (3.7), the relative reduction in via circuit inductance is:

$$\frac{\Delta L}{L_1} = -\frac{L_2}{L_1}\left[\frac{(2\pi f M)^2}{R^2 + (2\pi f L_2)^2}\right] = -0.01 \quad \text{at} \quad f = 1\,\text{GHz}$$

Similarly, the added resistance as a fraction of the original inductive reactance is:

$$\frac{\Delta R}{2\pi f L_1} = \frac{R}{2\pi f L_1}\left[\frac{(2\pi f M)^2}{R^2 + (2\pi f L_2)^2}\right] = 0.02 \quad \text{at} \quad f = 1\,\text{GHz}$$

For shorter via lengths or lower frequencies, these values are even smaller. Thus the presence of the terminated loop has a minimal effect on VDD/VSS via circuit impedance.

Finally, we need to look at the effect the presence of the 500 μm non-plated hole has on the impedance of the VDD/VSS plane pair. Keep in mind that the scale here is very small: less than 1 mm, so the one-eighth wave length frequency is ~20 GHz in FR4 material. Therefore, we cannot use a simple transmission line approach to assess

the effects. What we can do is use commercial field solver tools to examine the effect on the VDD via to VSS via impedance. Figure 3.9 shows two test structures used to examine the effect of the hole. Both consisted of 10 cm square, 18 μm thick VDD and VSS planes separated by an FR4 dielectric ($\varepsilon_r = 4$) and a single 250 μm diameter VDD via surrounded by four 250 μm diameter VSS vias at a 1 mm pitch. As shown, these vias were surrounded by industry standard 760 μm (30 mils) diameter anti-pads as required to prevent shorting. The first structure contained only vias and anti-pads, while the second structure contained a 760 μm anti-pad for the probe hole, located between VDD via A and VSS via B.

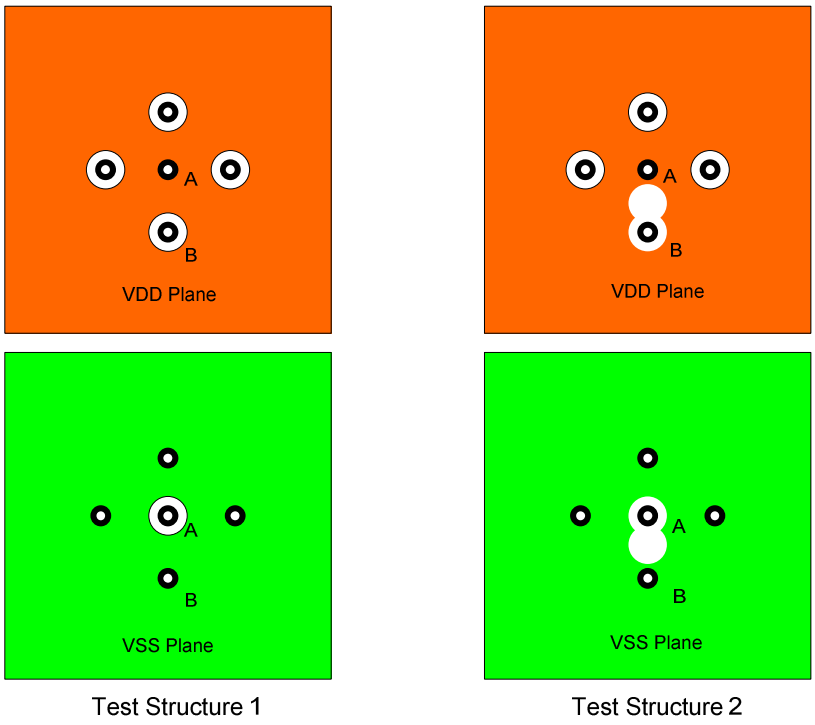


Figure 3.9 – Plane Impedance Test Structures

Two commercial simulation tools, PowerSI® and PowerDC®, both from Sigrity Inc., were then used to calculate the impedance seen looking into vias A and B and the DC resistance between these vias. For the AC test, two different plane separation distances were tested: 51 μm (2 mils) and 102 μm (4 mils). For the DC resistance calculation, a voltage source was connected between the VDD and VSS planes at a point collinear

with vias A and B, 4.5 cm from via A and 4.4 cm from via B. The change in impedance over the frequency range of 10 MHz to 1 GHz produced by the presence of the probe hole was imperceptible, as was the change in DC resistance.

Chapter 4

Initial Measurements

From the preceding design analysis, it appears that a single turn induction loop can be a practical sensor for measuring AC currents in printed circuit board vias. What we must do now is demonstrate, using a real sensor, that we can accurately measure AC via currents. In the process, we should also validate the basic conclusions of the preceding section regarding magnetic field fall-off with distance. The final test is to determine if the values of $\partial I/\partial t$ in real printed circuit boards are actually measurable. Two sets of tests were conducted to answer these questions. In the first, we developed a fixture to provide a "best case" measurement environment to test the basic ideas. In the second test, we created a loop probe which would work in a modern printed circuit board and modified a board from a high end Ethernet router to allow it to be inserted between power and ground vias under BGA packages to make current measurements. The remainder of this chapter details the methods and results of these two tests.

4.1 First Test: An SSTL Registered Buffer

In this first test, a commercially available 14 bit registered buffer with SSTL2 outputs created the currents for measurement. This made it easy to create a known pattern of activity. By measuring the voltage across the SSTL2 output termination resistors, the true output currents could be determined. The accuracy of the magnetic measurements of output currents could then be checked by comparison to these known values. Long vias were used to allow use of a relatively crude probe and to allow easy manipulation of the probe around the vias. The principal goals of this test were to

verify the expected magnetic field behavior in the vicinity of the vias and to show that via currents can be accurately measured using an inductive loop. An additional goal was to measure the break frequency of the loop. This frequency is fixed by the loop self inductance, which is proportional to loop area. The loop used was relatively large: 1 mm × 1mm. Therefore, if its break frequency equaled or exceeded the desired value of 1 GHz, the same should be true for a smaller loop that could be inserted in a real printed circuit board.

4.1.1 Test Fixture Description

To create a known pattern of electrical activity, the circuit shown in Figure 4.1 was used. All 14 outputs of a 74SSTL16857 registered buffer were terminated through 50Ω resistors to 1.25V, half the value of the 2.5V core (VDD) and output (VDDQ) supply levels. This established a symmetric output voltage swing about 1.25V and a symmetric output current swing about zero. A frequency dividing D flip flop drove all 14 inputs to the buffer so that all of the buffer outputs toggled simultaneously at half the rate of the buffer input clock. Separate clock inputs were provided for the buffer and the D flip flop, and these were driven by a dual output pulse generator. The two clocks could be separately enabled or simultaneously enabled at the same frequency with a phase difference between 0 and 360 degrees. This allowed the affects of the buffer clock and the data inputs on VDD supply current to be independently examined.

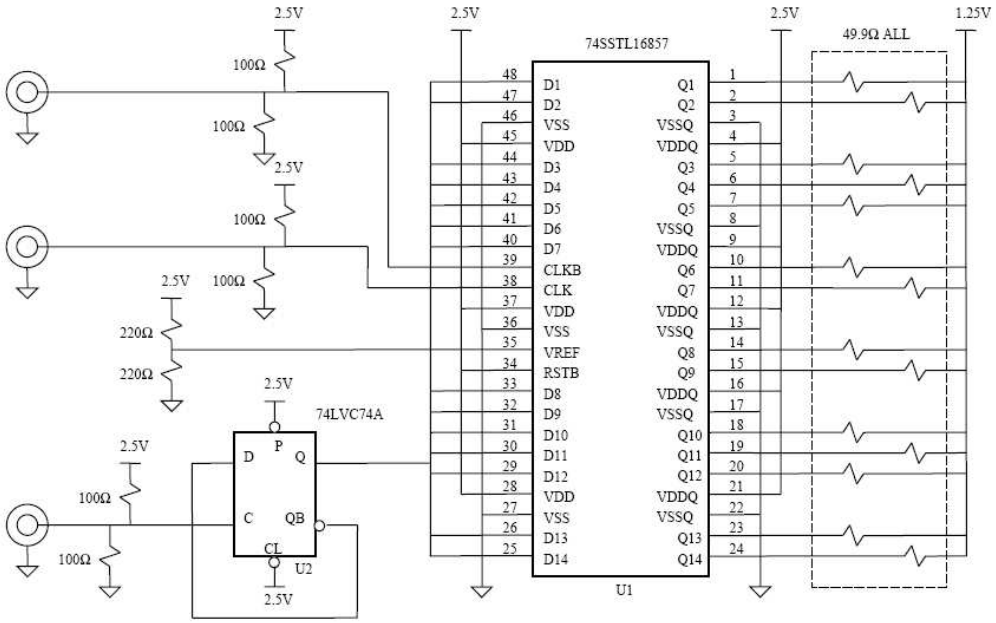


Figure 4.1 – Test Fixture Schematic Diagram

To effectively use the circuit of Figure 4.1, a fixture had to be designed which would emulate the vias found in typical printed circuit boards while allowing insertion and manipulation of a loop probe. Also, the probe had to be easy to construct. The resulting design is shown in Figure 4.2 and Figure 4.3. The 74SSTL16857 buffer, U1, was mounted on a 0.8 mm thick interposer board. To create an array of industry standard vias, the pins on each side of U1 were connected with surface traces to a double row of 250 μm (10 mil) diameter wire columns connecting the interposer board to a four layer base board. These columns emulated the industry standard 10 mil diameter vias used under BGA packages. The double row allowed easy access to all vias, and the 1.27 mm × 1.27 mm spacing used is a via pitch used under some BGA packages. A 1.5 mm air gap was maintained between the boards, and this allowed insertion of a 1 mm square induction loop. The back of the interposer was a ground plane, and the base board contained 2.5V and ground planes with the ground plane facing the interposer. The output terminating resistors were placed on the back of the base board.

Finally, a loop probe was created by winding a single turn of #28 AWG magnet wire around a 1 mm square wooden mandrel. A 50Ω coaxial cable with a 0.8 mm outside diameter carried the induced loop voltage signal out of the fixture. Precision XYZ translation stages were used to manipulate the probe. The current signatures of all vias were acquired by positioning the loop at the surface of each via and recording the loop output voltages. These voltages were measured using a Tektronix 7704B real time sampling oscilloscope, which had a 50Ω input impedance, a 20 G/sec sampling rate, and a 7 GHz front end bandwidth. The digitized data were exported for subsequent analysis.

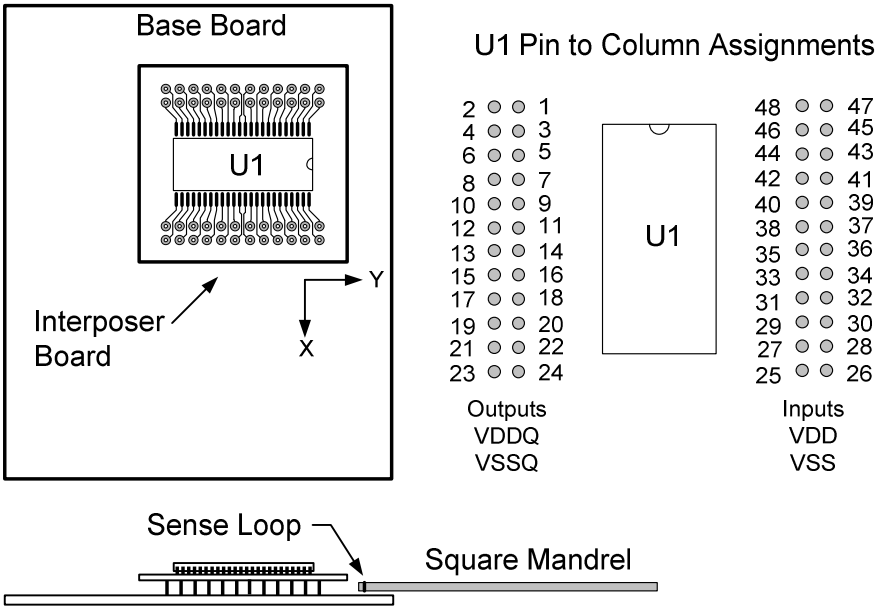


Figure 4.2 – Test Fixture Assembly Drawing

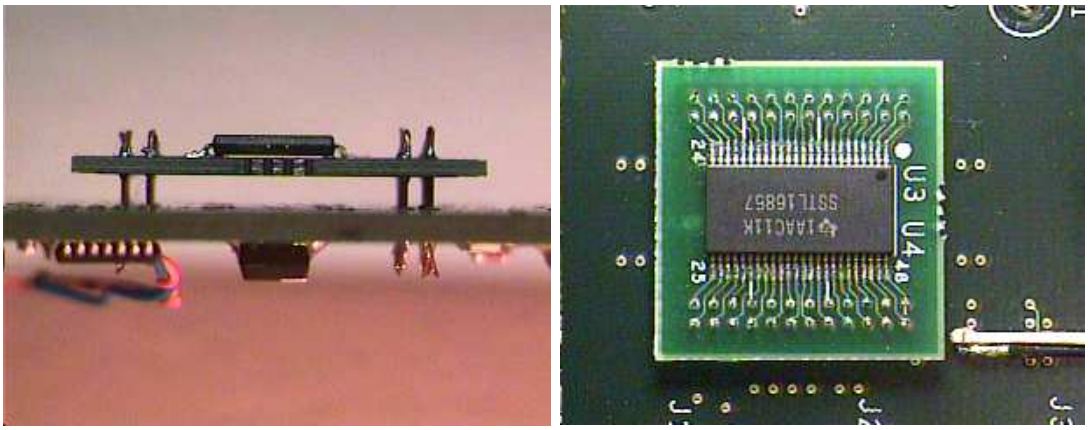


Figure 4.3 – Photograph of Test Fixture

4.1.2 Measurement Methods and Results

As discussed in Section 3.3, the location of the induction loop break frequency relative to the desired measurement upper limit determines how the loop output voltage data must be processed to recover via currents. Thus the first task was to determine the frequency response of the induction loop probe. This was done by driving the loop probe with an identical loop and using a vector network analyzer to measure S21 from the driving to the receiving loop. The result of this measurement is shown in Figure 4.4. It's clear from this result that the break frequency was 2 GHz, so the loop output voltage was proportional to dB/dt for excitations at and below this frequency. As a cross check, a TDR was used to measure the self inductance of the loop. The value measured was 3.9 nH. With a 50Ω termination, this gives an R/L break frequency of 2.04 GHz, which agrees well with the VNA measurement. Since the break frequency exceeded the minimum required upper measurement limit of 1 GHz, current measurements were obtained by numerically integrating the loop output voltage data and scaling the results by the calculated mutual inductance between the vias and the loop. The resulting upper measurement limit was 2 GHz.

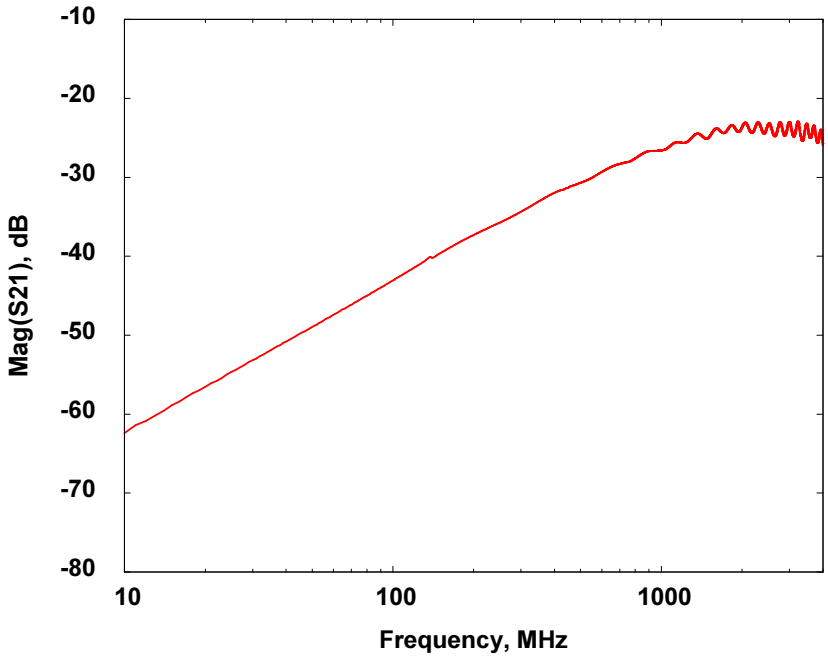


Figure 4.4 – Frequency Response of 1 mm Square Probe

In order to calculate the mutual inductance between a via and the loop, the decrease in magnetic field intensity with distance from the via must be known. The analysis of Section 3.1 predicts that the field intensity should be proportional to the inverse of this distance. A simple test was conducted to validate this prediction. With the data inputs to U1 static, U1's internal clock tree alone generated sufficient current to produce measurable loop signals at VDD/VSS vias 45/46 (see Figure 4.2). The loop output voltages obtained are shown in Figure 4.5. The signals were very nearly mirror images of each other, indicating that the via currents were of equal magnitude and opposite polarity. Since the surrounding data input vias were quiescent, vias 45 and 46 formed an isolated current doublet. The field surrounding this doublet was then used to measure the decrease in field intensity with distance. Figure 4.6 shows the measured peak loop output voltage (and therefore magnetic field) fall-off with distance both in and perpendicular to the plane of the doublet, normalized to the surface of via 45. Also plotted in the figure is the theoretical near field response. As can be seen, the fall-off exhibited near field behavior in both cases.

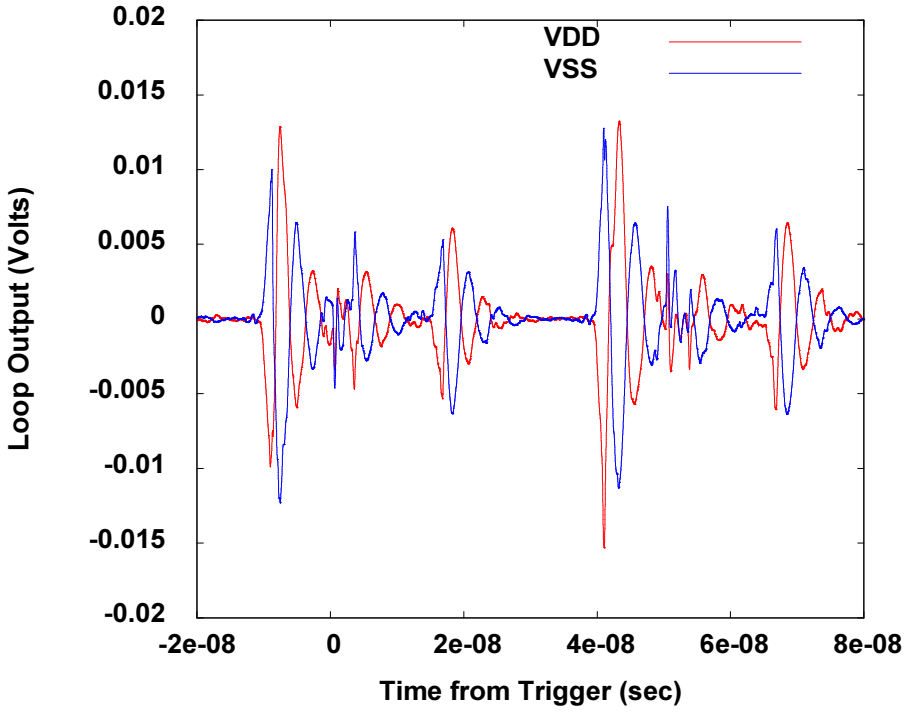


Figure 4.5 – Loop Output Voltages for VDD/VSS Vias 45/46

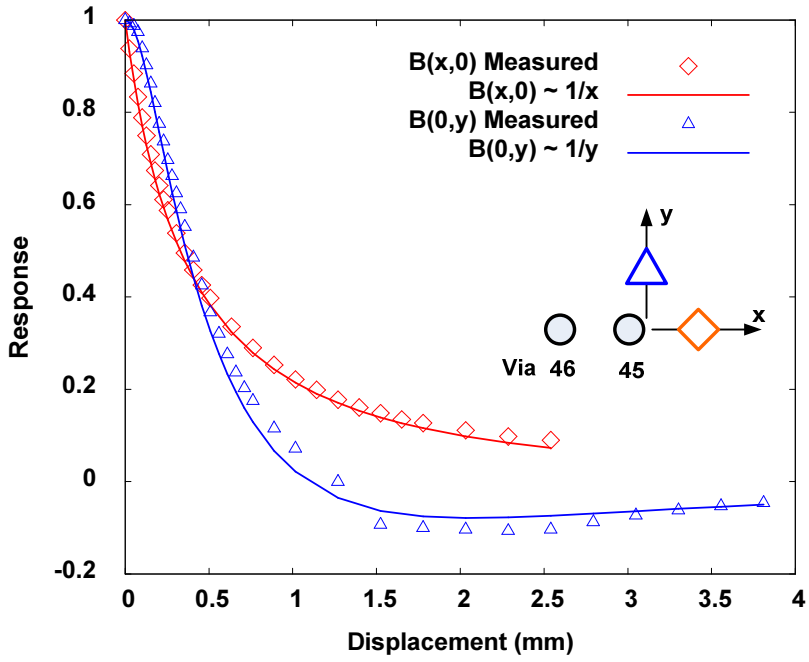


Figure 4.6 – Field versus Distance

With the field fall-off behavior verified, a via to loop mutual inductance of 480 pH was calculated, and initial measurements of output pin currents were attempted. The results showed that there was significant interference from the VDDQ and VSSQ vias embedded in the output via field. To remove this interference, the matrix, **M**, of mutual inductances between each measurement location and vias 25 through 48 (see Figure 4.2) was calculated using equation (3.2) of Section 3.1. The maximum distance involved was 15.3 mm. This was less than one-eighth of a wave length at 1 GHz, so quasi-static conditions were assumed. Measurements were made at each of vias 25 through 48 giving a voltage vector. This vector was pre-multiplied by the inverse of the mutual inductance matrix and integrated with respect to time to recover the vector of individual via currents. The sign convention adopted was that current out of the buffer pins was positive. The results for the output pin currents are shown in Figure 4.7, plotted in red. The known output currents obtained from voltage measurement across the terminating resistors were all within 2% of each other and are plotted in blue in the figure. The magnetic measurements for vias 6, 10, 15 and 19 showed a systematic error of 20% while the errors in the remaining measurements were 10% or less. The average error for all 14 outputs was about 10%. U1 was housed in a lead frame package and emitted significant EMI, similar to that described by Dong et al. [DDH04]. A large magnetic field component of these emissions was parallel to the interposer ground plane. Since this plane was of finite extent, circulating currents developed which allowed the field to leak through, creating the systematic measurement error. Modern BGA packages use planes to distribute power and microstrip or stripline traces to distribute signals, so these packages emit minimal amounts of EMI.

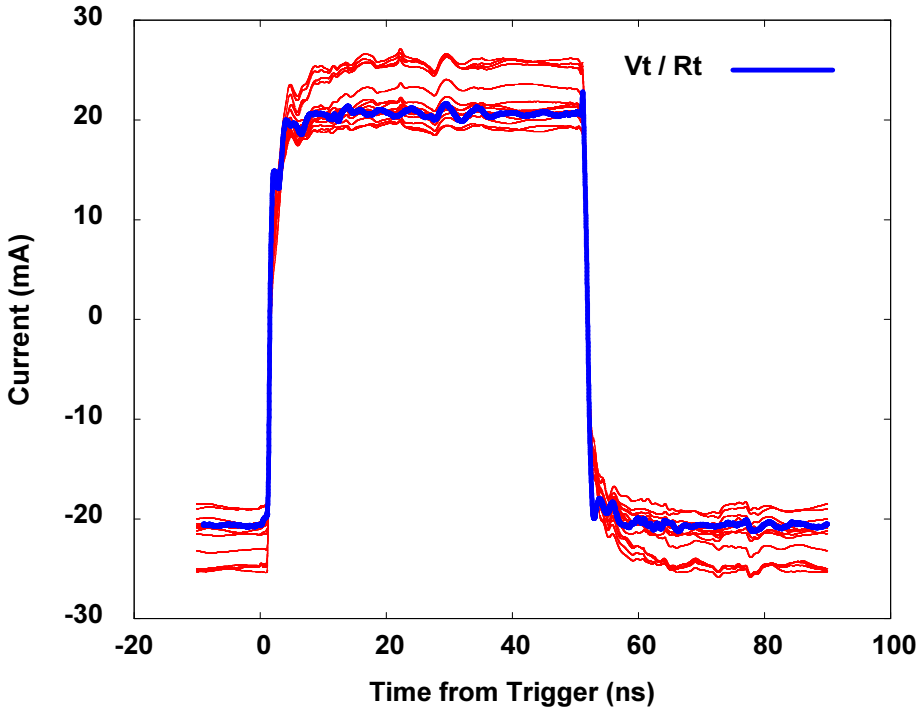


Figure 4.7 – Output Pin Current Measurements

Figure 4.8 and Figure 4.9 show the current measurements obtained for the VDDQ and VSSQ pins, respectively. Note that since the buffer output switching activity was well understood, the DC levels of the VDDQ and VSSQ currents could be restored. At each of the points labeled A and B in Figure 4.8, the sum of VDDQ currents is within of the sum of the actual output pin currents (14 × –21mA = –294 mA), while at point C the VDDQ current sum is within 5% of the correct value of zero. At each of the points labeled A and C in Figure 4.9, the sum of VSSQ currents is within of the sum of the actual output pin currents (14 × 21mA = 294 mA), while at point B the sum is within 5% of the correct value of zero. Overall, the measurement accuracy was reasonably good.

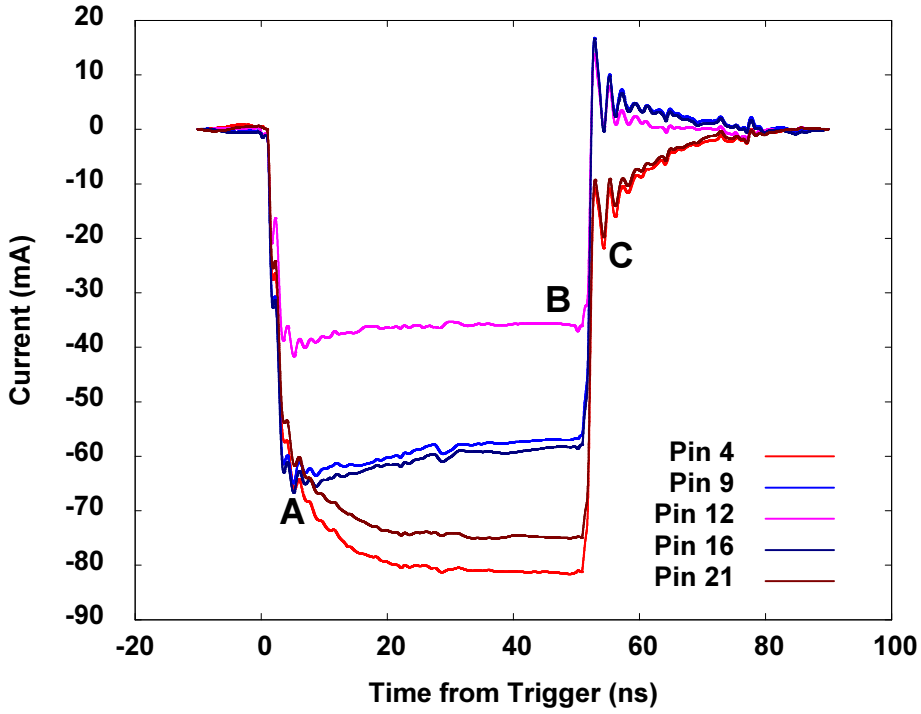


Figure 4.8 – VDDQ Pin Current Measurements

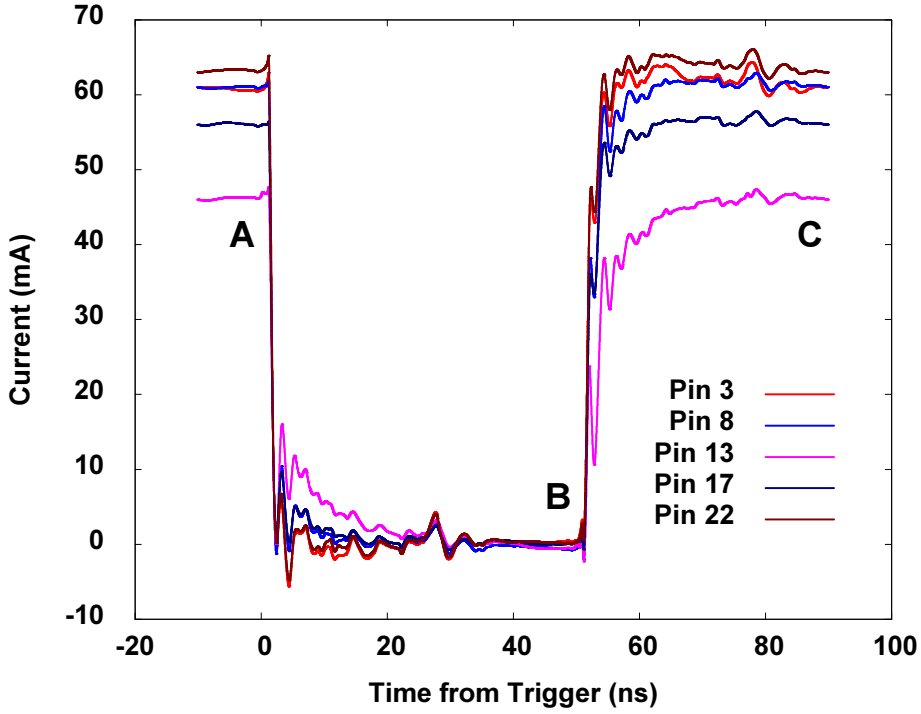


Figure 4.9 – VSSQ Pin Current Measurements

4.2 Second Test: A Commercial Ethernet Router Board

The results of the first test were encouraging: the loop probe had an upper measurement limit of 2 GHz, and signal and supply currents were successfully measured. The questions then were how to insert a loop between VDD and VSS vias in a real printed circuit board and what were the minimum detectable currents. To answer these questions, a second set of tests was conducted. We constructed a planar loop which would fit into a non-plated hole drilled between two vias in a printed circuit board, and modified a board from a high-end commercial Ethernet router was then modified to include 80 of these measurement sites distributed under 4 different BGA packages. A probe calibration site was also created. After determining the measurement bandwidth of this new probe, we used it to make measurements at all 80 sites with Ethernet traffic passing through the router. The overall goal was to demonstrate that via currents could be successfully measured in a real environment.

4.2.1 Description of Test Fixtures

The first task was to create a practical induction loop and a workable method for inserting it into an industrial printed circuit board (PCB). Standard PCB technology was used to create the loop which consisted of a 76μm (3 mil) wide copper trace on a 100μm (4 mil) thick FR4 substrate. Square pads at the end of the loop allowed attachment of a 50Ω semi-rigid coaxial cable. To create an insertion site, a 500μm (20 mil) diameter non-plated hole was drilled between power and ground via pairs. A diameter of 500μm is the largest that can be reliably drilled between vias at a 1mm spacing, which is the most common BGA ball pitch. Since the analysis of Section 3.2 showed that a via pitch to loop width ratio of 4 gave a good compromise between signal sensitivity and insensitivity to positional misalignment, the loop internal width was made 250μm (10 mil). The loop height was 3 mm, but the effective loop height for sensing is the distance from the top surface of the board to the supply/ground planes for the power/ground vias being measured. This was either 1.4 mm or 2.6 mm, depending on the voltage level measured. Figure 4.10 shows a drawing of the probe

and insertion method, and Figure 4.11 shows the probe in use. The measurement sites were distributed under 6 BGA packages and across four supply voltage levels, ranging from 1.0 to 2.5 volts. In all cases, measurement sites were placed between a supply and ground via pair. The increase in power/ground plane porosity resulting from insertion of these sites was less than 6% by area under any package.

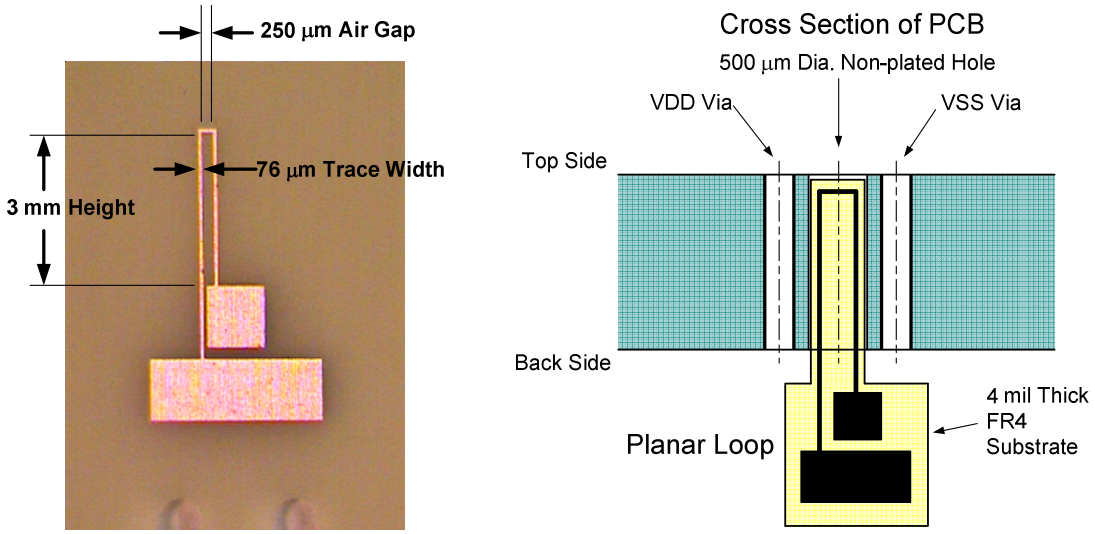


Figure 4.10 – Planar Loop and Insertion Site

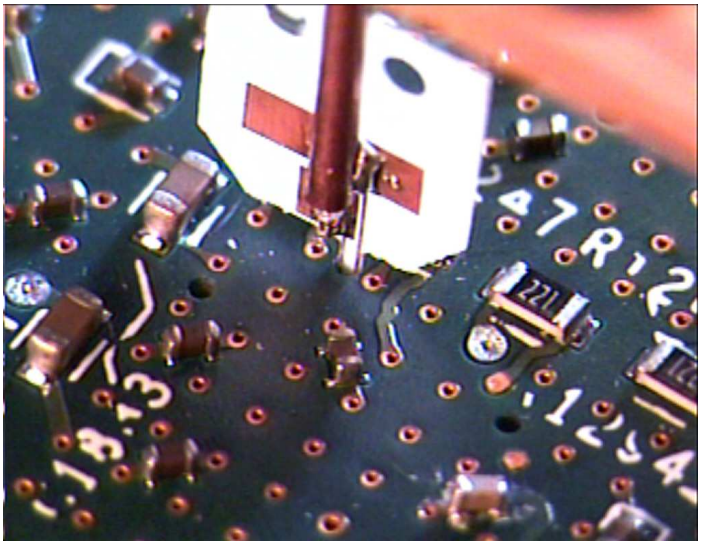


Figure 4.11 – Planar Loop Insertion in PCB

4.2.2 Measurement Methods and Results

The break frequency of the loop was found using the same method as in the first test. The loop was excited by an identical loop, and a vector network analyzer was used to measure S21 from the driving to receiving loop. The results are shown in Figure 4.12. The indicated break frequency was approximately 3 GHz. TDR measurement gave a loop self inductance of 2.6nH, giving an R/L break frequency of 3.06 GHz. These values agree relatively well with the simple analysis of Section 3.3. Since this break frequency exceeded the minimum required upper measurement limit of 1 GHz, current measurements were obtained by numerically integrating the loop output voltage data and scaling the results by the calculated mutual inductance between the vias and the loop. Thus the resulting upper measurement limit was 3 GHz, corresponding to a rise time of approximately 120ps. Since power distribution networks contain extensive charge storage capacitance, this was considered to be an adequate upper limit.

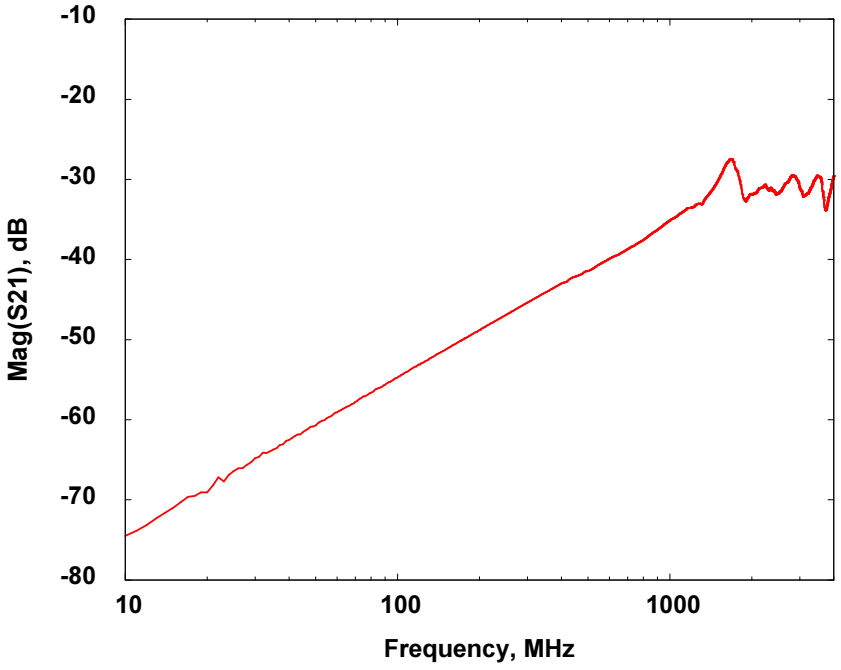


Figure 4.12 – Planar Loop Frequency Response

In addition to this upper measurement limit, a practical lower limit exists. This limit is reached when the loop output voltage can no longer be distinguished from the noise in the measurement instrumentation. To determine this limit, as well as to reconfirm the one-over-distance magnetic field fall-off, a calibration site was included in the router's printed circuit board. This consisted of two vias spaced at 1mm pitch with a 500μm diameter probe hole between them. The PCB stack-up was unaltered in this location, so the vias pierced but did not connect to the 14 power and ground planes of the board. Top surface traces routed at right angles to the line joining the vias allowed connection of a coaxial cable, and bottom surface traces also routed at right angles to the line joining the vias allowed connection of a 50Ω surface mount resistor across the bottom end of the vias. Figure 4.13 shows a drawing of the calibration site. A signal generator created a 10 mA amplitude sinusoidal current through the resulting circuit. A mutual inductance of 600pH from vias to loop was calculated assuming a one-over-distance field behavior, and loop output voltages were numerically integrated and scaled by this value to recover current waveforms. The loop voltage measurement device was the same Tektronix 7704B oscilloscope used in the first test (see Section 4.1.1).

Initial measurements showed the zero input signal noise in the oscilloscope to be well described by a normal distribution. Therefore, for repetitive signals, averaging should improve the overall signal to noise ratio by sqrt(N) where N is the number of samples averaged. Experimentation showed that using 2048 averages, a 100kHz 10mA current could be recovered with good accuracy. This corresponds to a peak $\partial I/\partial t$ of 6μA/ns. For single shot acquisitions, a frequency of 5 MHz would be required, corresponding to a peak $\partial I/\partial t$ of 0.3 mA/ns. Again, these results agree reasonably well with the predictions of Section 3.3. Finally, measurements were made at 1 MHz and at 10MHz to check the flatness of the response, and the results are shown in Figure 4.13. As predicted by the simple analysis of Section 3.2, the response was flat from 10 MHz down to 100 kHz. The amplitude values obtained were all within 2% of the correct value of 10mA.

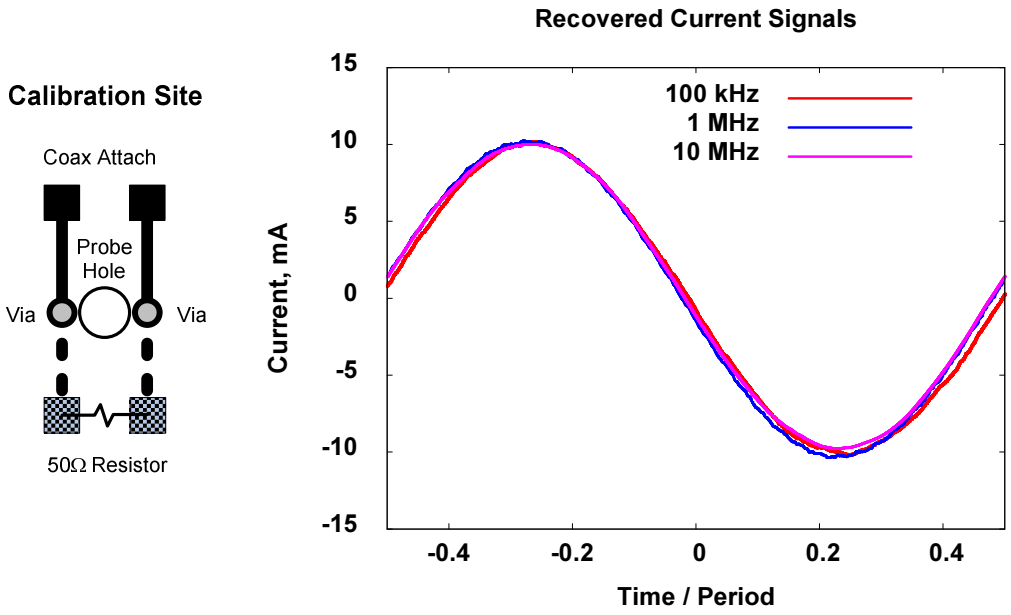


Figure 4.13 – Calibration Site and Recovered Current Signals

With the measurement limits of the probe determined, current measurements were made at the sites on the modified Ethernet router board. Output voltages of 2mVpp or greater were found at all sites. As an example, Figure 4.14 shows the measured current signature of a VDDQ pin of a content addressable memory (CAM) as 37 outputs switched simultaneously from low to high. The output resistance of the drivers and the PCB trace impedance were both 50Ω, and there were a total of 7 VDDQ pins at 2.5 volts. The receivers presented approximately a 4pF load at the output end of the lines. The calculated peak current was (37/7) × (2.5/100) = 132mA. Magnetic crosstalk was minimal at this site, and the measured peak current matches this value. As another example, Figure 4.15 shows the current signature of a core VDD (1 volt) pin of this same CAM with Ethernet traffic circulating. Figure 4.16 shows the distribution of peak VDD values for ten VDD pins distributed across the area of the package. Two loops were used: one to provide a stable trigger from one site and one to sample the remaining nine sites. Similarly clean measurement results were found at all 80 sites.

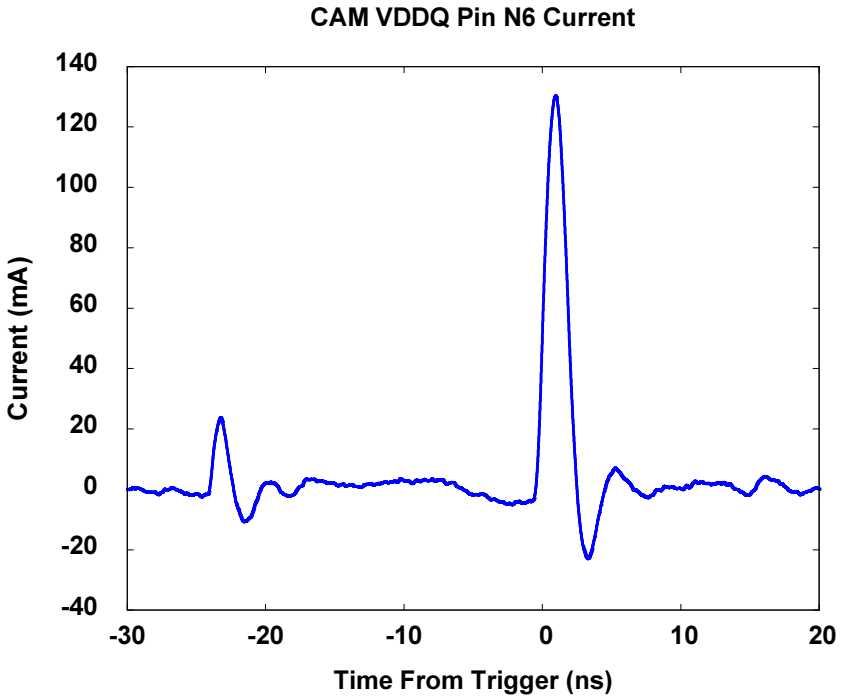


Figure 4.14 – Measured CAM VDDQ Pin Current

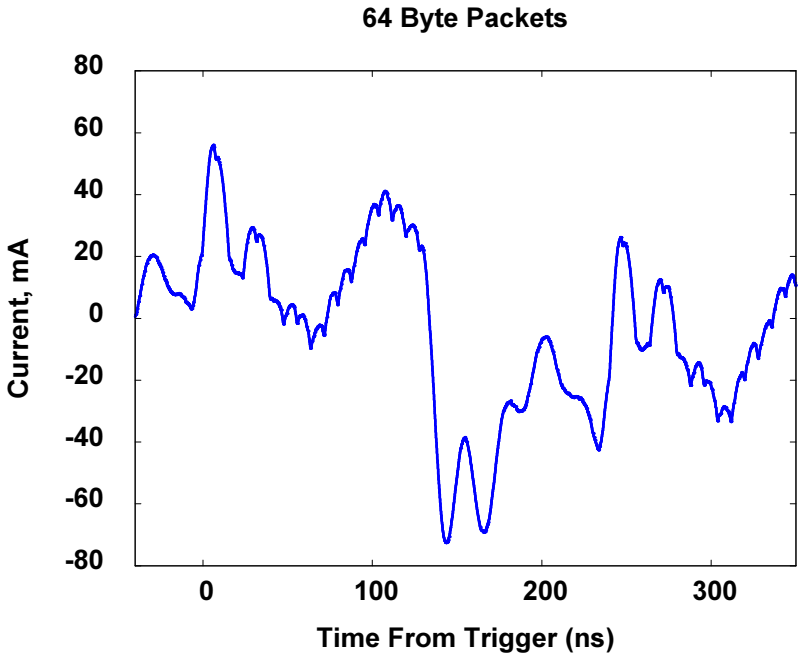


Figure 4.15 – Measured CAM VDD Pin Currents

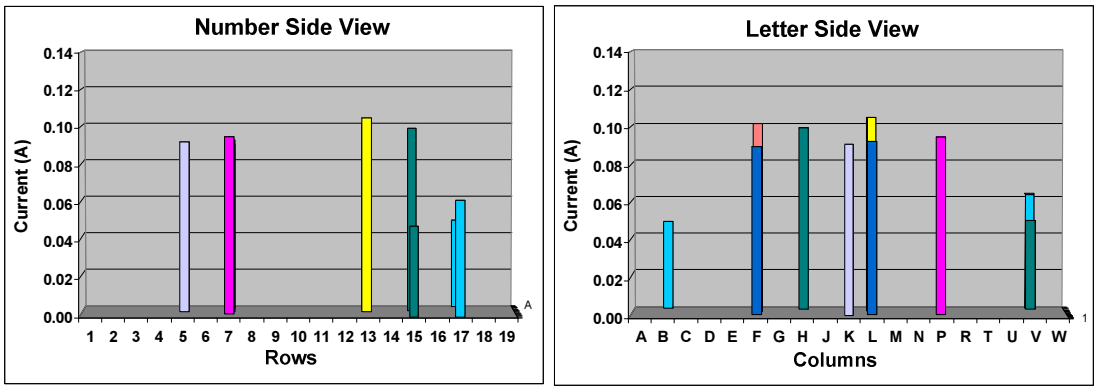


Figure 4.16 – CAM VDD Pin Current Distribution Across Package

Finally, measurements of the VDD and VDDQ via current signatures of this CAM were used to examine the validity of the assumption that power/ground plane pairs make no contribution to the induced loop voltage and also to examine the effect of bypass capacitors under the CAM. In both cases, the test procedure was the same: the peak loop output voltage was measured as a function of loop insertion depth, measured from the back side of the printed circuit board. In other words, the loop voltage was measured as a function of loop height, *h*. Figure 4.17 shows the measurement results for the 1V VDD/VSS via pair and Figure 4.18 the results for the 2.5V VDDQ/VSSQ via pair, normalized to full insertion amplitude. Neither via pair had bypass capacitors connected to them. For the VDD/VSS via pair, the results show the expected behavior with depth, and the indicated VDD/VSS plane pair position was ~1.8 mm from the top surface of the board, which is reasonably close to the actual value of 1.4 mm. There was some extraneous signal at 0.6 mm depth, and this was exactly the depth of the VDDQ/VSSQ plane pair. This implies that this plane pair did make some contribution to the loop signal, but the contribution was less than 10% of the total. The results for the VDD/VSS via pair also showed the expected linear behavior with depth, and the indicated VDD/VSS plane pair position was ~2.8 mm from the top surface of the board, which is quite close to the actual value of 2.6 mm. On balance, the assumption that plane pairs produce a negligible signal is reasonable.

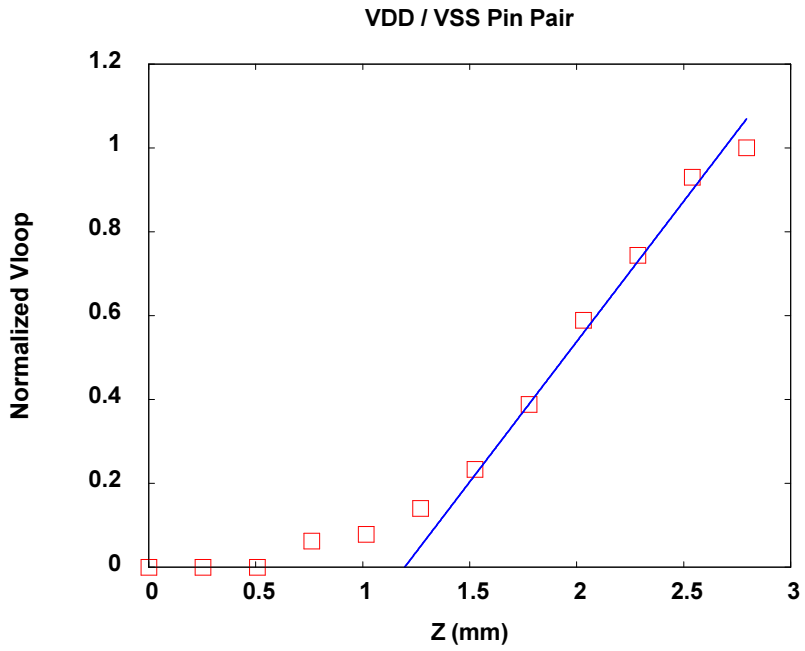


Figure 4.17 – Peak Loop Voltage vs. Insertion Depth for VDD/VSS

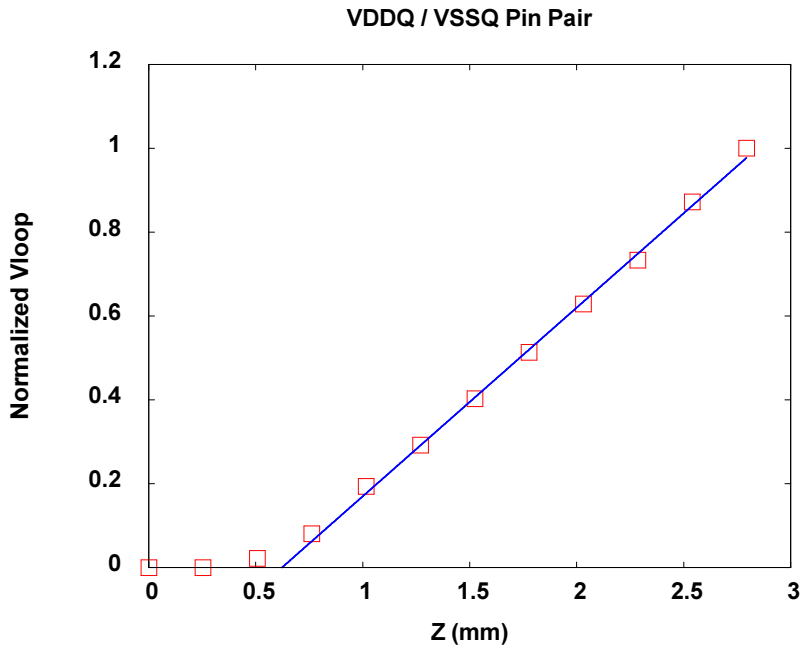


Figure 4.18 – Peak Loop Voltage vs. Insertion Depth for VDDQ/VSSQ

To investigate the effects of bypass capacitors, measurements were made on three VDD/VSS via pairs, each with 0.1μF ceramic bypass capacitors attached. The pairs were located near the center of the package area. Figure 4.19 shows the results. Note that for all three sites, the slopes of the initial linear segments are the same. Since the electrical environments for all three sites were similar, this implies that the all three bypass capacitors contributed nearly the same current. Then at ~1.6 mm depth, which is the location of the VDD/VSS plane pair, the slopes of the line segments change. The slope for VDD via L7 increases, indicating that the VDD plane is contributing current, whereas for VDD via V15, the slope decreases which indicates that some of the bypass capacitor current is passing into the plane. For VDD via V17, the slope remains unchanged, implying that the bypass capacitor contributes the entire VDD pin current. These results suggest that we can obtain data on the bypass capacitor currents as well as the package pin currents, an idea we will pursue in Chapter 5.

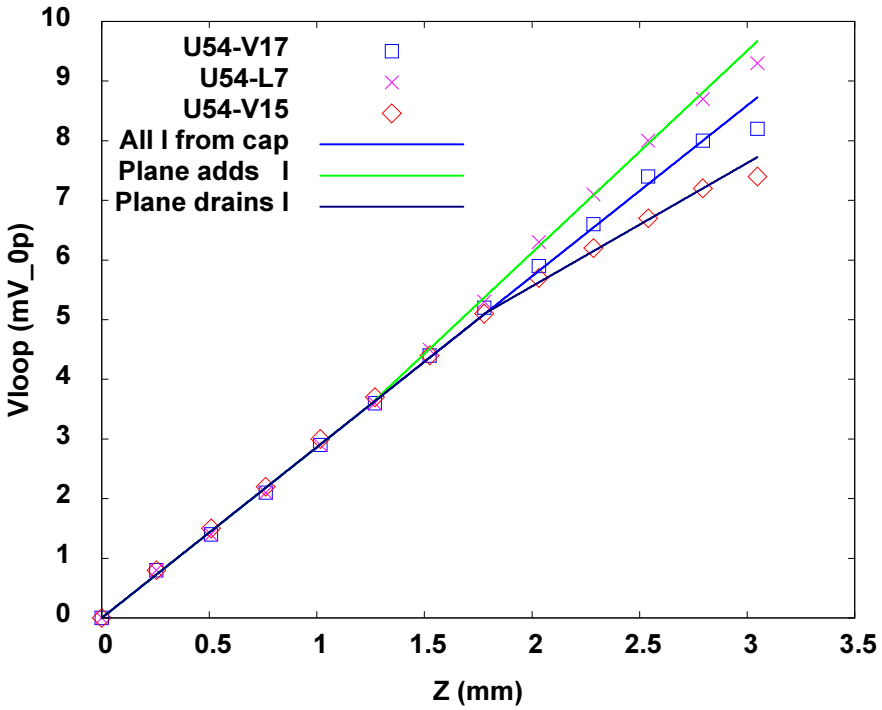


Figure 4.19 – Effect of VDD Bypass Capacitors

4.3 Summary

Taken together, the results of these two tests show that small induction loops can be used to measure transient currents flowing through power and ground vias in real printed circuit boards. Using standard PCB lithography, planar loops can be constructed which are small enough to fit between vias spaced at 1mm pitch under BGA packages and which provide a measurement bandwidth in excess of 2 GHz. When such loops are inserted between a power/ground via pair, the resulting sensitivity is approximately 0.2 mV/mA/ns per millimeter of current carrying via length. This allowed a repetitive current of 6μA/ns in a 3mm long via pair to be measured with high fidelity using an industry standard sampling oscilloscope. In a board from a high end Ethernet router, 80 sites under BGA packages yielded clean measurements. Where magnetic crosstalk from adjacent vias was minimal, the measured current signatures matched expected current values to within 5% error. For VDD pins of a CAM memory, activity dependent transient current patterns were observed, and the distribution of peak intensities of these patterns across the package was measured. Furthermore, varying the effective loop height by varying loop insertion depth validated the treatment of power/ground planes as parallel plate waveguides for transient signals and also allowed the current contributions of bypass capacitors to be investigated. Overall, the measurements could be used to validate simulation results, since crosstalk effects can be accounted for in simulation.

Chapter 5

An Application Example

The results thus far show that power system currents in printed circuit boards can be measured using an inductive loop sensor. Such loops can be made small enough to be inserted into real printed circuit boards and yet have a bandwidth and sensitivity adequate to sensing power network currents. Furthermore, the measurement accuracy is reasonable; errors in the five to ten percent range can be expected. We will now apply this technique to a real world problem and demonstrate that useful results can be obtained. While there are many possibilities, a problem of major concern for system designers is that of large integrated circuits with very large changes in switching fraction. Such parts can exhibit large swings in supply current and also very large values of $\partial I/\partial t$. The power system must be designed to supply adequate charge, both instantaneously and on a sustained basis, or the supply voltage will droop excessively, leading to compromised performance or outright failure.

Critical aspects of this are the selection and placement of bypass capacitors to provide transient charge and the number, thickness, and placement of supply and ground planes. As discussed in Chapter 2, simulation of the power networks is a critical part of this process. For system designers, however, the simulation and design problems are compounded by the fact that vendors of integrated circuits are often either unable or unwilling to provide comprehensive data on the temporal and geometric distribution of supply currents. This forces designers to apply estimated "worst case" stimuli in simulation. It is then uncertain whether the resulting design is adequately robust. If the supply pin currents of problematic parts could be measured during realistic worst case operation, this uncertainty could be removed. This is the

task addressed in this chapter. We will measure the currents in all power and ground pins of a large integrated circuit as this part makes worst case transitions in internal activity. The results will show the distribution of current as a function of time and the actual values of $\partial I/\partial t$ that reach the printed circuit board. In addition, we will see that it is possible to measure currents in both bypass capacitors and supply planes as well, giving additional insight into the performance of the power network.

5.1 Description of the Approach

The integrated circuit selected for test was a Content Addressable Memory (CAM), which is frequently used in Ethernet routers. This section describes the methods used to obtain maps of the real time supply currents for this device. The characteristics of the CAM are described in section 5.1.1, along with the reasons for choosing this device. Section 5.1.2 then describes the test printed circuit board used to take the current measurements. Finally, section 5.1.3 describes the methods used to collect and process the measurement data.

5.1.1 The Test Device

As already stated, a Content Addressable Memory (CAM) was used as the test device. This device was chosen for several reasons. First, this type of memory can exhibit large swings in supply current to the memory core. Besides read data and write data modes, a CAM has a search mode. In this mode, a data key is presented to the CAM inputs, and the contents of the memory are searched for stored data matching the key. If a match is found, an index to the location of the matching data is placed on the outputs. The search mode is implemented by placing a match line across each row of cells in the memory mat. The match lines are all driven high at the beginning of a search. The input key data are then compared to the bits in each row, and if any of the bits in a row differ from the key, the match line for that row is pulled low and a miss is said to occur. Thus, large currents can be drawn during compares that end in a miss. Depending on the size and organization of the memory mat and on the sequence and

rate of application of keys, very large and abrupt changes in supply current can occur. The memory chosen had a storage capacity of 10 Mb, operated synchronously from a 500 MHz clock, and had a 1 volt core supply voltage. Thus this part is a good example of the kind that present power system design challenges to system engineers.

A second reason for selecting this particular CAM was that it contained built-in self test (BIST) logic capable of executing a number of different test patterns. After the BIST logic is configured and triggered, no further manipulation of chip inputs is required for test execution. This significantly simplified the test board: only a small field programmable gate array (FPGA) was required to control the BIST tests. Also, the BIST logic could be configured to loop on a particular test. This allowed for data averaging which improves the signal to noise ratio. One of the BIST tests was specifically designed to create worst case values of $\partial I/\partial t$ by alternating between large numbers of consecutive misses and large numbers of consecutive matches. It is this test that was used to create the supply currents for measurement. The algorithm for the test is described in the following pseudo-code:

```
Initialization {
     write_ones_to(all_locations);
     write_zeros_to(last_row_of_all_blocks);
     enable(all_blocks);
     set_search_width_to(all_bits);
}
Test {
     For(specified_loop_count) {
          search_for(all_zeros, n times);
          search_for(all_ones, n times);
     }
}
```

Finally, the CAM chosen was contained in a 576 ball BGA package with an organic substrate and a 1 mm ball pitch. The package technology is thus a present day standard, and the size is large enough to present power design challenges. This becomes clear when looking at the part's pin-out, shown in top view in Figure 5.1, (horizontal pin numbering follows the industry standard practice: A B C D E F G H J K L M N P R T U V W Y). Here, the 1 volt core VDD pins are shown in red and the

VSS pins in blue. As can be seen, VDD and VSS pins are distributed across the package area, but their density is high in a “hot spot” in the center of the package, under the die. This is typical for large BGA packages. Supplying current to this hot spot is a preoccupation of PCB designers because their presumption has always been that this is the area through which the majority of the supply current passes. Yet, as can also be seen, doing this is complicated by the large number of intervening pins. In contrast, pins away from this area have traditionally been viewed as less effective in supplying power. Using the chosen CAM, with the pin-out of Figure 5.1, will allow these assumptions to be quantitatively evaluated.

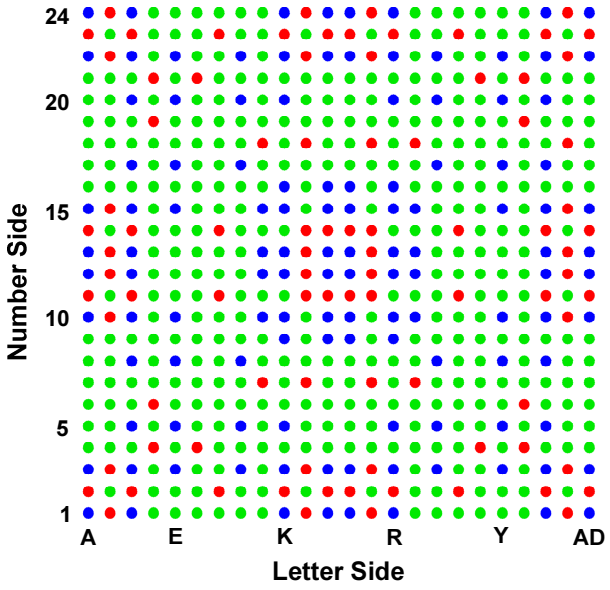


Figure 5.1 – Top View of Test CAM Package Pin-out

5.1.2 The Test Board

With the test device (hereafter referred to as the DUT) selected, it was then necessary to produce a test board which would simultaneously provide a realistic system environment and also allow the currents of all of the DUT package pins to be measured. A block diagram of the resulting design is shown in Figure 5.2. The BIST control pins of the DUT were driven by an FPGA; the FPGA was programmed and controlled via an IEEE/ANSI 1149 standard JTAG bus. Since most of the DUT inputs

were unused for BIST testing and the DUT was designed to allow cascading, most of the outputs were conveniently terminated by connecting them back to the inputs. The few remaining outputs were terminated resistively. The output loads were thus typical of those seen in a real system environment. An on-board clock generator provided a 500 MHz clock to the DUT and a 250 MHz clock to the FPGA phase aligned with the 500 MHz clock. The JTAG inputs were synchronized to the 250 MHz clock inside the FPGA. Thus the operation of the FPGA was synchronized to that of the DUT. In addition to controlling the BIST logic, the FPGA emitted a trigger output whose transition could be precisely aligned to the start of the BIST test in the DUT. This allowed data from multiple measurements to be coherently merged. Finally, on-board DC-DC converters provided all supply voltages, including the 1V DUT core supply.

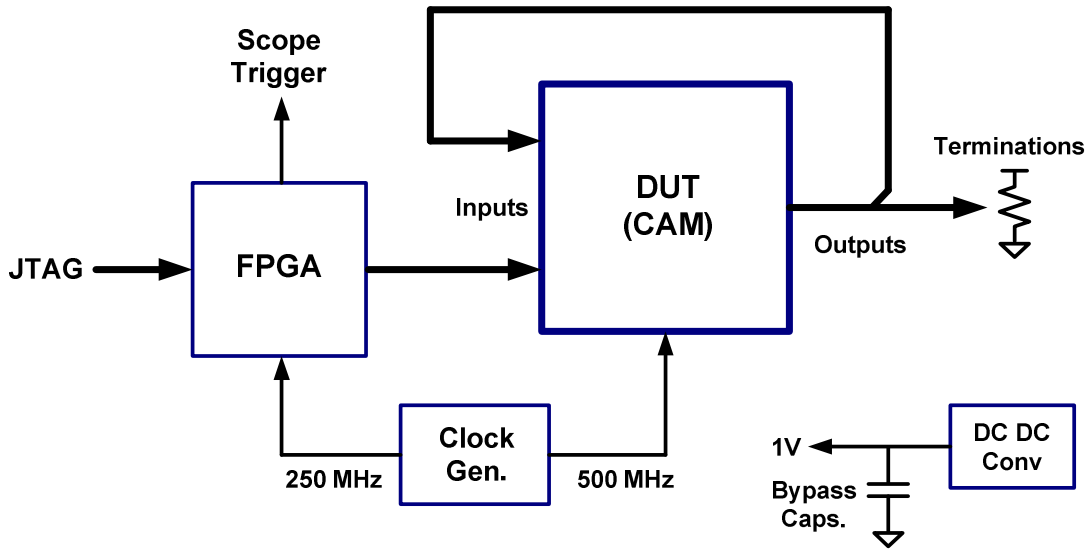
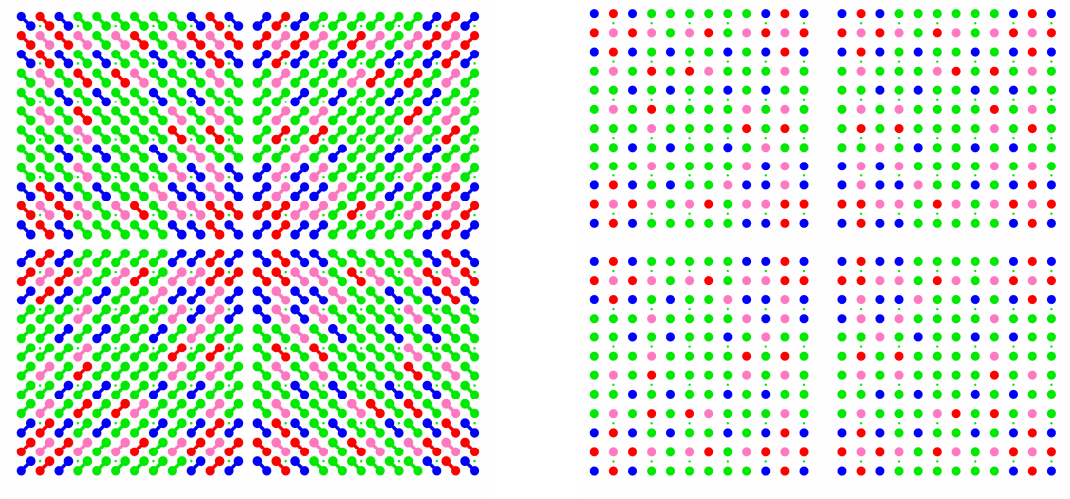


Figure 5.2 – Test Board Block Diagram

Standard printed circuit board practices were followed to create the footprint for the DUT on the test board as shown in Figure 5.3 (a). Surface mount pads of 500 μm diameter were placed at 1 mm pitch to create a 24 square array of 576 contact points for the BGA package of the DUT. Then 250 μm O.D. vias were placed interstitially with the surface mount pads, and short surface traces joined pad to via. The vias were place so as to create chevrons pointing diagonally away from the center of the

package. The via pattern thus created, shown in Figure 5.3 (b), results in 2 mm wide "ways" clear of obstructing vias. This is a practice commonly used by board designers to clear the way for current to the presumed hot spot at the center of the package. Following the procedure described in Section 4.2, insertion sites for the inductive loop were created by placing 500 μm diameter non-plated-through holes next to the vias. In this case, we need to have a measurement site for each of the 576 vias. This allows magnetic crosstalk from neighboring vias to be removed, as described in the next section and the current in each via to be determined.



(a) (b)

Figure 5.3 – Footprint and Via Field under DUT

Placing a measurement site between every via, however, would significantly increase the porosity of the area under the chip and could thus excessively disturb the impedance of the power/ground plane network. To avoid this, four DUT footprints were placed on the test board, each with 144 measurement sites. These footprints were identical in every way (bypass capacitor placement, IO loading, etc) except for the placement of the probe holes. In the first footprint, the measurement sites were placed between every other via (i.e. on a 2 mm pitch), both vertically and horizontally, starting 0.5 mm above the upper left had corner via in Figure 5.3 (b). In the second footprint, this pattern was slipped down one via pitch vertically. In the third footprint,

the initial pattern was slipped down one via pitch vertically and to the right one via pitch horizontally. In the fourth footprint, the initial pattern was slipped one via pitch to the right. Thus for each footprint, the space between vias in the vertical direction was unobstructed, and in the horizontal direction, only every other space was occluded. The resulting increase in porosity was under fifteen percent. By taking measurements at the 144 sites in each footprint and moving the DUT through all four footprints, measurement data for all pins could be acquired. To enable this, SK0576BG2701A compression sockets from DCI Corporation were used to connect the DUT to the test board. These sockets are used on high performance integrated circuit testers for IC characterization and have an extremely low profile and therefore low inductance. Compressible pins are used to make the PCB to IC connection, and when the part is fully seated, 2.6 mm of height is added. Using equation (3.8) in Section 3.4 and the stack-up dimensions for the board, the sockets add 1.3 nH of inductance for an adjacent core VDD/VSS via pair. This was deemed a tolerable disturbance. The validity of this assumption will be addressed during the discussion of measurement results in Section 5.2.

To produce an environment typical of systems in which the DUT is used, the layer stack-up of the printed circuit board was made identical to the supervisor board of a high performance Ethernet router. The board contained 24 layers: 8 stripline signal layers, 8 ground planes to form the striplines, and 4 supply/ground plane pairs. Total board thickness was 3 mm (116 mils), and the VDD/VSS plane pair for the DUT core power was located 1.4 mm (55 mils) below the front (DUT attach) side of the board, which is the same position these planes occupy on the Ethernet router board where the DUT is used. Appendix A contains full documentation of this stack-up.

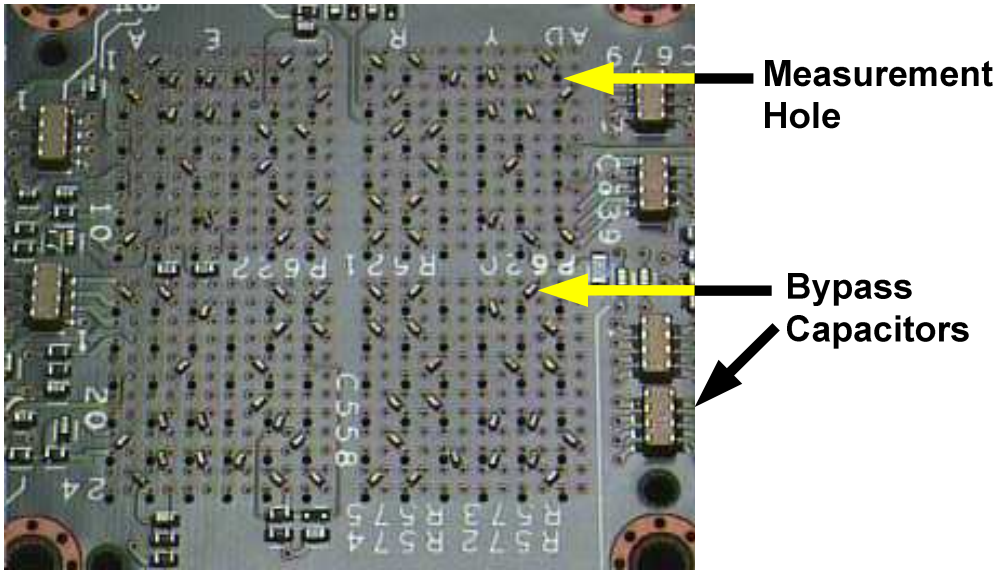


Figure 5.4 – Test Board Bypass Capacitor Placement

Bypass capacitors were placed on the back side of the board. The capacitance values and placement of these capacitors closely matched the implementation on Ethernet router supervisor boards were the DUT is used. The majority of the bypass capacitors used were 0.1 µF ceramic capacitors with an X7R dielectric and a 0201 case size. These were placed diagonally across core VDD and ground vias as shown in Figure 5.4 (the measurement site holes are also visible in this figure). Low inductance 8 pin 2.2 µF IDC ceramic capacitors were placed at the edge of the via array. At the corners of the via array 100 µF ceramic capacitors (not shown) were placed to provide bulk charge storage. During testing, the worst case supply noise observed at the DUT was 10 mV peak to peak, so this bypass strategy was more than adequate for this application.

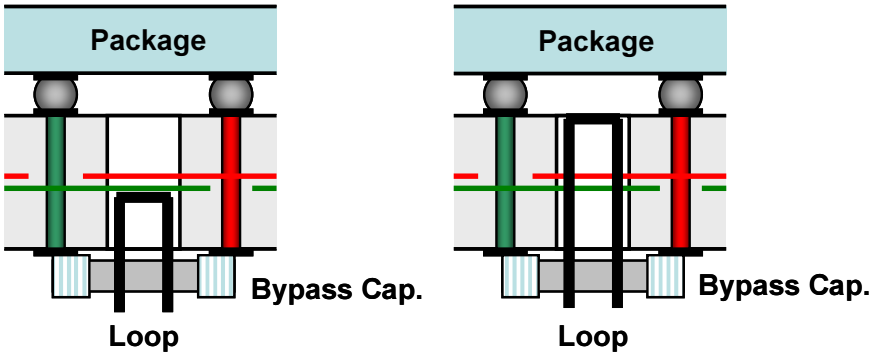
5.1.3 Measurement Methods

Since measurements were taken at multiple sites distributed across four distinct footprint locations, we must have a stable reference point in time if we are to be able to coherently combine the measurements and make sense of the results. This was accomplished by using an FPGA operating synchronously with the DUT to set up and

initialize BIST tests in the DUT and to provide a trigger of data collection (see Figure 5.2 above). The logic inside the FPGA would watches the BIST commands being sent to the DUT, and when the `start_bist_test` command is recognized, an "offset" counter is started. When this counter reaches a preset value, the FPGA pulses its trigger output, and a "cycle" counter is started. When this counter reaches a preset value, another trigger pulse is issued and the counter is reset to zero and begins counting up again. By setting the cycle counter to the length of the BIST test loop, the offset counter could be used to both skip over the BIST initialization sequence and position the trigger at a predetermined location within the test. For the results discussed in this chapter, the trigger was placed at the beginning of the BIST test loop and remained constant for all data measurements. A Tektronix TDS 7704B sampling oscilloscope was then used to measure the output of the inductive loop at each measurement site. Samples were collected at 8 ps intervals, and acquisition was initiated by the FPGA trigger pulse. The presence of a stable trigger also allowed signal averaging to be used. At each measurement site, sixteen samples of data where collected and averaged. This improved the signal to noise ratio by a factor of four, which was more than adequate.

The induction loop sensor used in these measurements was the same as that used in the initial testing described in Section 4.2 and was inserted into the measurement sites from the back side of the printed circuit board as shown in Figure 4.11 of that section. This creates both a problem and a data collection opportunity. When the loop is fully inserted in the printed circuit board next to either (or both) a VDD of ground pin, the induced loop voltage will be the sum of that created by currents into the package pin(s) and that created by currents through any bypass capacitors attached to the vias on the back side of the board. Since there is an intervening power/ground plane pair which can either source or sink current, the value of the package pin current is indeterminate. To solve this problem, the approach shown in Figure 5.5 was taken. For each measurement site, two readings were taken: one with the loop half-way inserted, just up to the core VDD/VSS plane pair, and one with the loop fully inserted.

The package pin current data are then obtained by subtracting the first reading from the second.



(a) Half Insertion (b) Full Insertion

Figure 5.5 – Loop Positions for Measurements

While somewhat tedious to execute, this method provides us with more information about the behavior of the power network. The half insertion measurements, if carefully executed, allow the transient currents in the bypass capacitors to be determined, which in turn allows a quantitative assessment of their effectiveness to be made. Furthermore, recalling the results of Figure 4.19 in Section 4.2.2, we can obtain information about the plane currents by subtracting two times the half insertion data from the full insertion data. If the result is zero, then the entire package pin's current is supplied or sunk by the attached bypass current. A positive result indicates that the plane is supplying current and a negative result that it is sinking current. All of these data can then be plotted against the pin location to give the distribution of these currents across the package area as a function of time.

To obtain the current value for each pin from the loop voltage measurements requires that the magnetic crosstalk from adjacent vias be removed. Following the approach taken in Section 4.1, the vector **V** of voltage measurements can be expressed in terms of the vector **I** of via currents and the matrix **M** of mutual inductances between vias and measurement sites as: $\mathbf{V} = \mathbf{M}\frac{\partial}{\partial t}\mathbf{I}$. In general, the elements of these quantities are complex numbers, reflecting the phase effects of signal propagation over

distance. The problem becomes far simpler if we can assume quasi-static conditions, that is, that the phase effects of signal propagation over distance are minimal and can be ignored. The elements of **M** are then real numbers, and the current vector can be obtained as $\mathbf{I} = \mathbf{M}^{-1} \int dt\, \mathbf{V}$ using simple matrix algebra. To see if the quasi-static assumption can be made, first note that the supply/ground plane pairs form a parallel plate waveguide with spacing on the order of 100 μm and that the loop measurement bandwidth is 2 GHz. Therefore, the propagation mode for all measurable signals in the power system will be transverse electro-magnetic. Hence the propagation velocity will be independent of frequency and given by $v = c/\sqrt{\varepsilon_r}$ where *c* is the velocity of light in a vacuum and ε_r is the relative dielectric constant of the insulating material between the power and ground plane. The test board used a fiber glass / FR4 resin composite which had a relative dielectric constant of 4. Setting a phase shift 10% of a period of as the limit for the applicability of the quasi-static approximation gives a distance limit of 7.5 mm at a frequency of 2 GHz. Since each measurement site is 0.5 mm from its target via and the field fall-off is one-over-distance, the magnitude of interfering signals will be reduced by a factor of $0.5/7.5 = 0.067$ at the quasi-static limit. For signals with a lower frequency, *f*, the distance limit increases by a factor of $\left(2 \times 10^9\right)/f$.

As we will see in the next section, the spectrum of the measured signals contained essentially no energy above 100 MHz. At this frequency, the distance is four times the diagonal length of the DUT footprint. Therefore, quasi-static conditions were assumed. The mutual inductance matrix could then be easily computed by repeated application of equation (3.2) in Section 3.1. Since the core power / ground plane pair for the DUT were located very near the center of the test board's thickness, the via height above and below the planes was essentially the same. Therefore, a single mutual inductance matrix can be used to recover both bypass capacitor and package pin currents. Equations (5.1) show the sequence of calculations used to recover current data. In these equations, V_{hi} are the voltages measured with the loop inserted half way into the board, and V_{fi} are the voltages measured with the loop fully inserted into the

board. **M** is the mutual inductance matrix, and $\mathbf{I_{cap}}$, $\mathbf{I_{pin}}$ and $\mathbf{I_{plane}}$ are the current vectors for the bypass capacitors, package pins and power planes respectively.

$$\mathbf{V_{cap}} = \left[\int V_{h1}dt \quad \ldots \quad \int V_{hn}dt\right] \qquad \mathbf{V_{pin}} = \left[\int\left(V_{f1} - V_{h1}\right)dt \quad \ldots \quad \int\left(V_{f1} - V_{hn}\right)dt\right]$$

$$\mathbf{I_{cap}} = \left[\mathbf{M}^{-1}\mathbf{V}_{\mathbf{cap}}^{\mathbf{T}}\right]^{\mathbf{T}} \qquad \mathbf{I_{pin}} = \left[\mathbf{M}^{-1}\mathbf{V}_{\mathbf{pin}}^{\mathbf{T}}\right]^{\mathbf{T}} \tag{5.1}$$

$$\mathbf{I_{plane}} = \mathbf{I_{pin}} - \mathbf{I_{cap}}$$

The TDS 7704B oscilloscope gives a column vector of voltage data versus time and it's because of this that the transpose operators appear in the equations. Also note that by assuming quasi-static conditions, we can do the time integration before solving for the currents. These integrations were done numerically, using the trapezoidal approximation, and the solutions for currents were done in MATLAB® using its left divide function. Finally, bear in mind that since the DC levels of the currents cannot be found using an inductive loop, the true values of the integration constants are unknown. Therefore, the trigger point for data acquisition was set to the end of the sequence of CAM matches (the minimum activity point), and the integration constant for all measurements was set to zero. This provided a consistent point of reference which allowed relative comparisons between the measurement data to be made.

5.2 Measurement Results

This section first describes the precursory measurements made to verify the behavior of the magnetic field surrounding the vias in the printed circuit board under the DUT. The second part then describes the results of applying the methods of the previous section to measuring current in the DUT package pins. As might be expected, a large amount of data resulted, which gave a current vs. time trace for each pin. While this data could be used in numerous ways, the discussion will focus on three areas of particular interest to system designers: the distribution of current across the package pin field, the effectiveness of bypass capacitors, and the maximum / minimum values of $\partial I/\partial t$ reaching the printed circuit board.

5.2.1 Field Measurement

Before taking current measurements, the blank test printed circuit board (i.e. the PCB without components attached) provided the opportunity to verify the one-over-distance fall-off of magnetic field strength in the via array under the DUT. A VDD and ground via were shorted together on the backside of the PCB, and a pulse generator in series with a 50Ω resistor drove current into the VDD via and out of the ground via on the front side of the board, creating a current doublet. Induction loop measurements were then taken at 5 sites, as shown in Figure 5.6 (Red = VDD, Blue = ground).

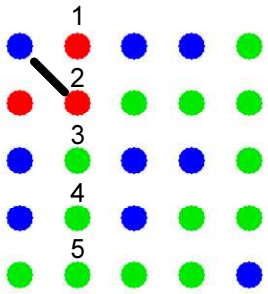


Figure 5.6 – Blank PCB Test Locations

The pulse generator emitted a 10 MHz trapezoid wave with a 1 volt amplitude and 0.8 ns rise and fall times; this created a $\partial I/\partial t = \pm(1/50\Omega)/0.8\text{ns} = \pm 2.5 \times 10^7$ A/sec in the via pair. The 250 μm wide inductive loop was inserted 2 mm into the board (mechanical interference with the shorting wire prevented full insertion). Using the values of W = 250 μm and h = 2 mm, the measurement results are predicted by recasting equation (3.1) to use the distances from the active VDD and ground vias, giving:

$$\frac{V}{V^*} = \ln\left[\frac{(2\chi_1+1)^2+(2\psi_1)^2}{(2\chi_1-1)^2+(2\psi_1)^2}\right] - \ln\left[\frac{(2\chi_2+1)^2+(2\psi_2)^2}{(2\chi_2-1)^2+(2\psi_2)^2}\right] \qquad (5.3)$$

Where: $V^* = \frac{\mu_o}{4\pi} h \frac{\partial I}{\partial t}$ $\chi = \frac{x}{W}$ $\psi = \frac{y}{W}$

Table 1 below compares the predicted and measured results. In this table, χ_1 and ψ_1 are the normalized *x* and *y* distances from the driven VDD via, and χ_2 and ψ_2 are the normalized *x* and *y* distances from the driven ground via. While there is some scatter in the measurement data, the agreement with prediction is reasonable. Differences are 800 μV or less.

Table 1. Field Fall-off Test Results

Location	χ_1	ψ_1	χ_2	ψ_2	Predicted V_{loop}	Measured V_{loop}
Site 1	–6	0	–2	4	–0.7 mV	–0.9 mV
Site 2	–2	0	2	4	–6.0 mV	–5.5 mV
Site 3	2	0	6	4	4.0 mV	4.8 mV
Site 4	6	0	10	4	0.8 mV	0.8 mV
Site 5	10	0	14	4	0.3 mV	0.3 mV

As a cross check to these measurements, a field simulation was run using the HFSS® three dimensional electromagnetic field solver from Ansoft Corporation. Two planes were spaced at 100 μm distance to form a parallel plate wave guide, and their edges were terminated with a perfectly absorbing layer. Two through-vias at 1 mm pitch pierced these planes and were driven differentially using 50Ω microstrip lines and HFSS wave-ports. To check for disturbance created by intervening signal and VDD vias, a three by three array of vias at 1 mm pitch was placed 1 mm from the driven pair. These vias were connected to the bottom plane but insulated from the top plane. Figure 5.7 shows the magnitude of the magnetic field along a line half way between two rows of signal vias. The simulated field intensities at 10 MHz, 100 MHz and 1 GHz are plotted along with the near field prediction. As can be seen, the simulation results for all three frequencies were essentially the same. The agreement with the near field prediction is reasonable but not perfect, indicating that the vias may have some effect; also, the simulation accounts for resistive losses in the copper planes, which the simple near field prediction does not.

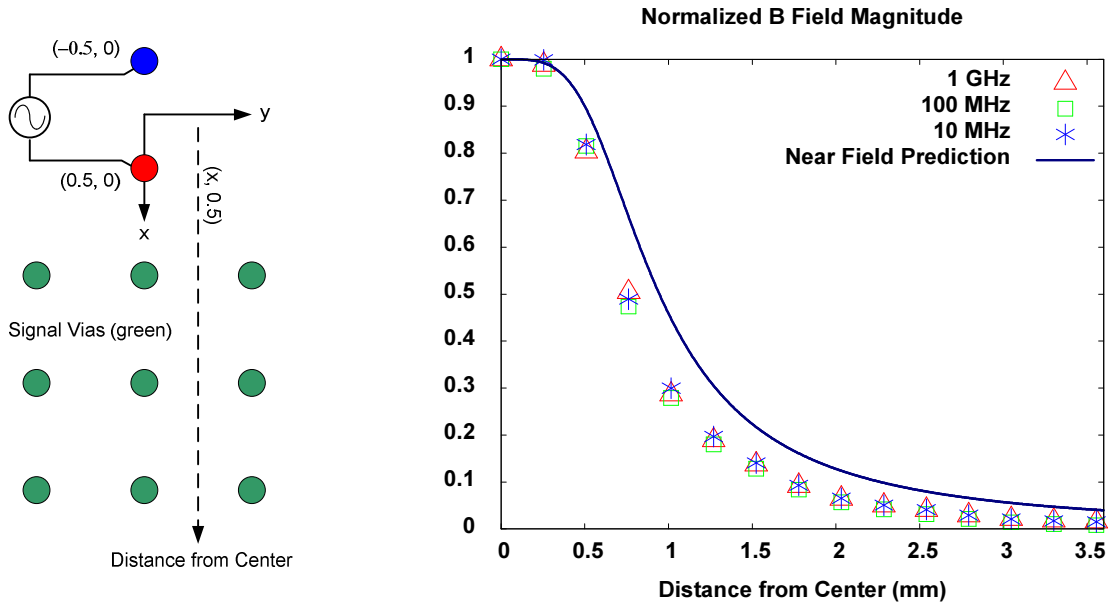


Figure 5.7 – Electromagnetic Field Solver Results with Signal Vias

To check the affects of ground vias, which short the ground planes together, we repeated the field simulation with the signal via array replaced by a three by three array of ground vias connected to both planes, once again on a 1 mm pitch. The results, shown in Figure 5.8 below, are similar to those for the signal via array, but some differences are present. For the 100 MHz and 1 GHz frequencies, there is some non-monotonic behavior of the field intensity near the first ground via. This suggests the presence of a low quality factor resonance in the ground via array. Deep into the block of vias, the field intensity falls somewhat more rapidly than in the previous case. For the 10 MHz frequency, the resonant behavior is absent, but again, the field intensity inside the ground via array falls off somewhat more rapidly than it does inside the block of signal vias. The conclusion has to be that ground vias do disrupt the magnetic field somewhat. Fortunately, as can be seen in the figures, the disruption occurs when the field intensity is low, limiting the error in assuming near field behavior, and except for the very center of the package the number of ground vias per unit area is low (see Figure 5.1). Therefore, we will assume that near field behavior applies to the magnetic field, but refinement of this treatment is an area for further work.

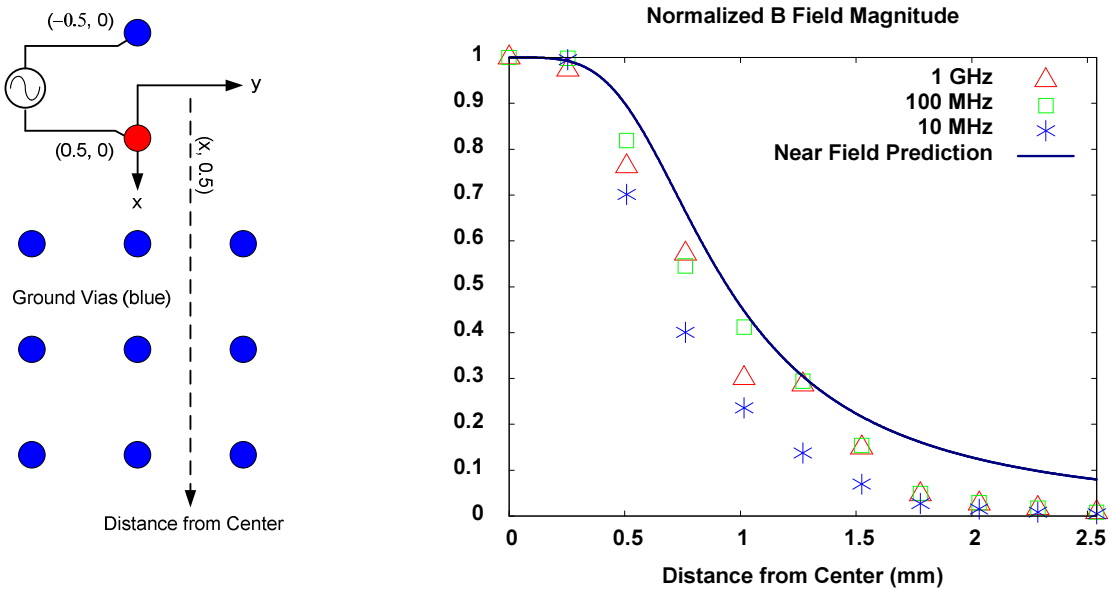


Figure 5.8 – Electromagnetic Field Solver Results with Ground Vias

5.2.2 Current Measurements

With the magnetic field behavior approximated as near field, the methods of Section 5.1.3 were then used to collect measurement data at all 576 via locations while the DUT executed the $\partial I/\partial t$ BIST test described in that section. This test executes internally in the DUT without any activity on the input or output pins, and the measurements showed that the input/output pins and their VDDQ and VSSQ supply pins were quiescent. Only the input clock pins and the 209 VDD and VSS core supply pins created transient current signatures. Data from these pins were processed according to the methods outlined in the previous section to yield a full mapping of the VDD and VSS pin currents over a test cycle. These results can clearly be used to validate the predictions of simulations as well as to provide measurement data to printed circuit board designers. As stated earlier, the focus in this work is on measurement data that will aid printed circuit board design.

To begin the discussion, we can get a good feeling for the overall supply current behavior, as well as a validity check on the results, by summing all the VDD pin currents and all the VSS (ground) pin currents and plotting the results versus time. Figure 5.9 shows just this plot. Note that in the sign convention adopted is that current *into* the package is positive. Thus ground current is negative. Looking at the figure, the overall current behavior during the BIST test is apparent. The test produces a square pulse of current with amplitude of about 12 amperes and duration of approximately 10 ns. The sharp rise in current occurs as the test progresses from a series of searches resulting in matches into a series that results in misses. The current then decreases to a value of 8 amperes and remains at this level for 240 ns. This is followed by a sharp drop in current as a sequence of matches begins. The sum of the VDD and VSS currents should, of course, be zero, and this sum is plotted in the figure. While not perfect, the sum is small; its maximum value as a fraction of VDD current during the miss sequence is 5 percent. The rapid oscillations in the waveform are most likely the result of ringing in the package, and have a frequency of approximately 48 MHz. The slow undulation in the VDD current results from ringing of the bypass capacitors, and has a frequency of 14 MHz. The rise and fall times are approximately 5 ns. Given this current behavior, we could then run another check on the results. The average supply current could be read from the DC-DC converters on the test board. The value obtained was 4.1 amperes. Given the 50% duty cycle of the VDD current square wave, this implies a peak current of approximately 8 amperes and a minimum current close to zero, values very close to those measured.

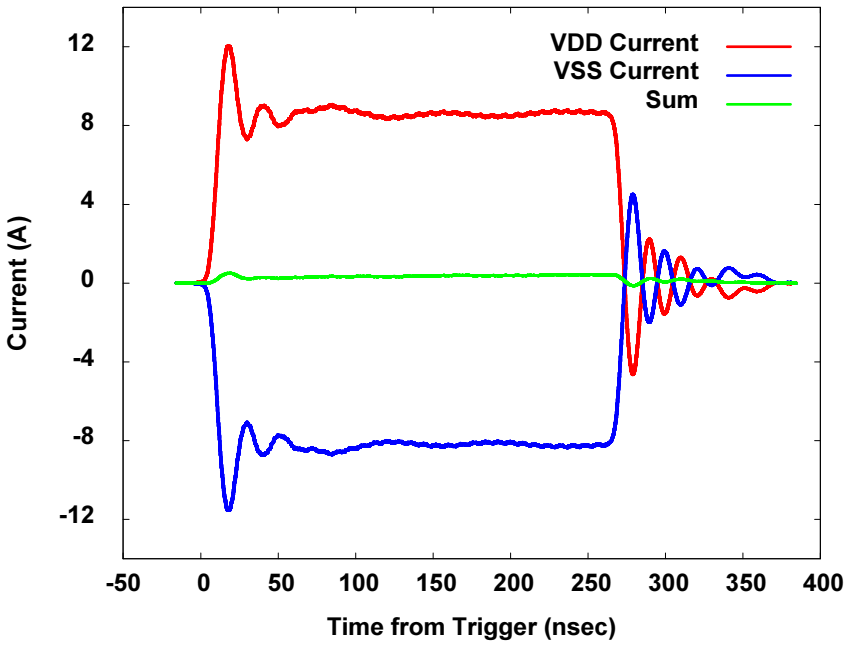


Figure 5.9 – Total VDD and VSS Currents

The general nature of the current distribution can be seen by plotting the value of the current for each of the pins across the two dimensional array of DUT package pins and then observing the evolution of this plot as a function of time. The resulting sequence for the VDD pin currents is shown in multi-pane Figure 5.16. This shows the currents just beginning to rise, at their maximum value, at their quasi steady-state values near the end of the miss sequence and the ringing after the falling edge. The time stamps shown are times from trigger shown in Figure 5.9. The corresponding sequence for the VSS pins is shown in Figure 5.17. For viewing clarity, the *negative* of the pin currents in plotted in this figure. After looking at these plots it is clear that both the VDD and VSS currents are larger in the center of the package, under the die. It is also clear, however, that significant current is carried by the peripheral pins outside this area. We can quantify the extent of this effect by calculating the average per pin current for pins inside the central area and the average per pin current for peripheral pins outside of this area, and then plotting these values as a function of time. Figure 5.10 shows the result for VDD pin currents. The central area is the area

inside the red square and contains 12 of the 89 total VDD pins. The plot shows that during the current peak, the average per pin current is 30 percent higher for pins in the central area than the average for peripheral pins. After the peak, during the period of 100 to 250 ns after trigger, this increases to 33 percent. Similar results were obtained for the VSS pins.

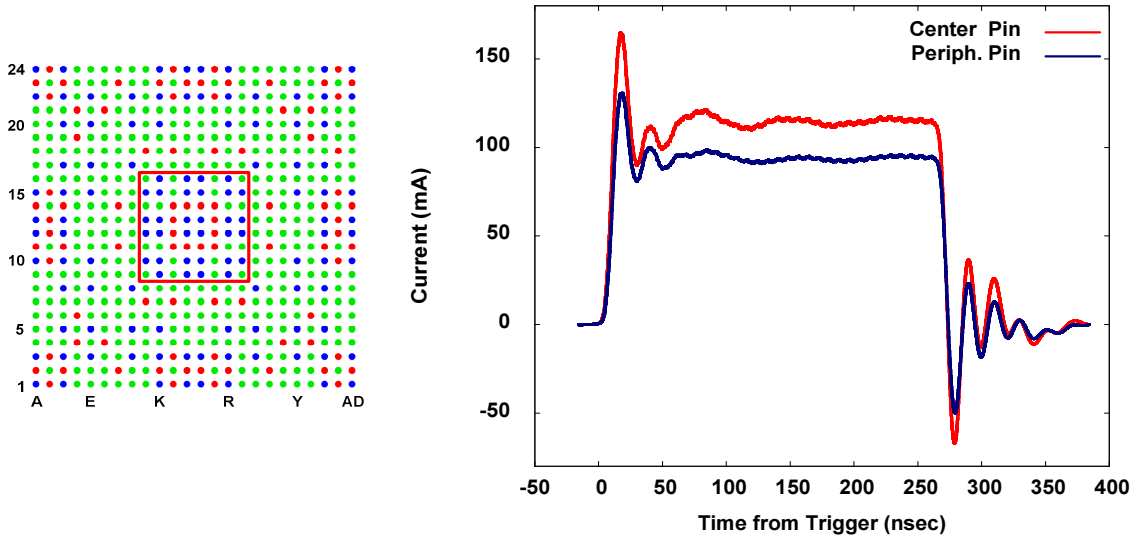


Figure 5.10 – Average Per Pin VDD Currents

Thus the current density is higher in the central area, and supplying power to this area is important. Board designers should note, however, that considerable total current can still be supplied by the periphery. In this case, for example, the periphery supplies 77% of the total current while the central area supplies the remainder. The DUT package is doing a reasonably good job of spreading the DC current load across the package area.

To examine the effectiveness of the bypass capacitors placed behind the DUT on the backside of the board, we can start by plotting the distribution of capacitor currents across the area of the DUT footprint as was done for the VDD and VSS pin currents. The result is shown in multi-pane Figure 5.18. The sign convention is that current *out* of the capacitors is positive, and the time stamps are the same as in Figure 5.16 and

Figure 5.17. It is clear that bypass capacitors make a large contribution of charge during the interval of peak current demand as the DUT transitions from matches to misses. Then when the DUT transitions from misses back to matches, the bypass capacitors absorb a large amount of charge as the current stabilizes. Between these events, the capacitors make no significant contribution to VDD pin current. Notice that the currents at the center of the left and right edges of the chip lag behind the other currents. This is where the 2.2 μF IDC capacitors are located (vs. 0.1 μF everywhere else), and the lag is consistent with their large value. By subtracting the capacitor currents from the package pin currents, we can display the contribution of the VDD plane to the package pins. This result is shown in multi-pane Figure 5.19, where the sign convention is that current from the plane to the pin is positive. The plot for the 16.792 ns time stamp, the point of maximum current draw, shows that the VDD plane makes very little contribution to the pins with bypass capacitors attached to their vias. After the peak passes and the current draw stabilizes, the plane contributes all of the current, which is clear from the plot with the 223.992 ns time stamp.

We can quantify the contribution of the bypass capacitors, and reveal something rather surprising, by displaying the currents of two adjacent VDD pins in the central area, one with a bypass capacitor attached and one without, and the bypass capacitor current on the same graph. The result is shown in Figure 5.11 (see Figure 5.10 for pin locations). Pin L11 (red trace) has a 0.1 μF bypass capacitor attached to its via while adjacent pin M11 (blue trace) does not. The current of the capacitor attached to L11 is shown with the green trace; the 14 MHz ringing results from a damped oscillation of the capacitor and supply/ground plane circuit. After the peak current draw, the currents in L11 and M11 converge to nearly the same value. During the peak current draw, however, the situation is quite different. While the current through pin L11 is 50 percent larger than the current through pin M11, more importantly, the bypass capacitor supplies 90 percent of pin L11's current. This is a general result. Figure 5.12 shows the current for each of the bypass capacitors as a fraction of the current of the package pin to which they are connected. There are two 3D plots: one looking from

the numbered side of the package and one looking from the lettered side of the package (see Figure 5.1). The smallest contribution (48%) is made by the 2.2 μF low inductance capacitor placed outside of the DUT footprint and connected to the pin via by wide traces. For capacitors placed inside the DUT footprint and connected directly to the pin via, the smallest contribution is one at 72%; the remaining contributions are 80% or more. Only four values, however, are over 120%. These four pins have currents very much smaller than those of their neighboring VDD pins. This tight bound implies that the capacitors primarily supply the pins to which they are attached.

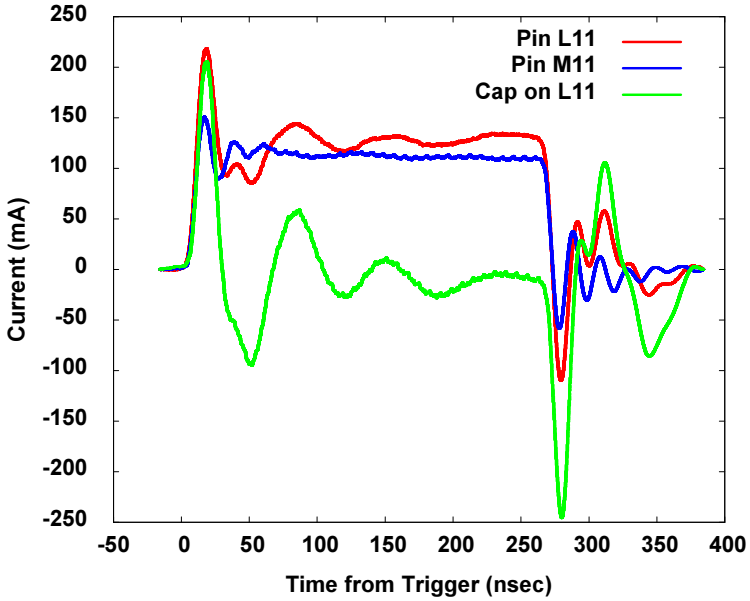


Figure 5.11 – Bypass Capacitor Current Contribution

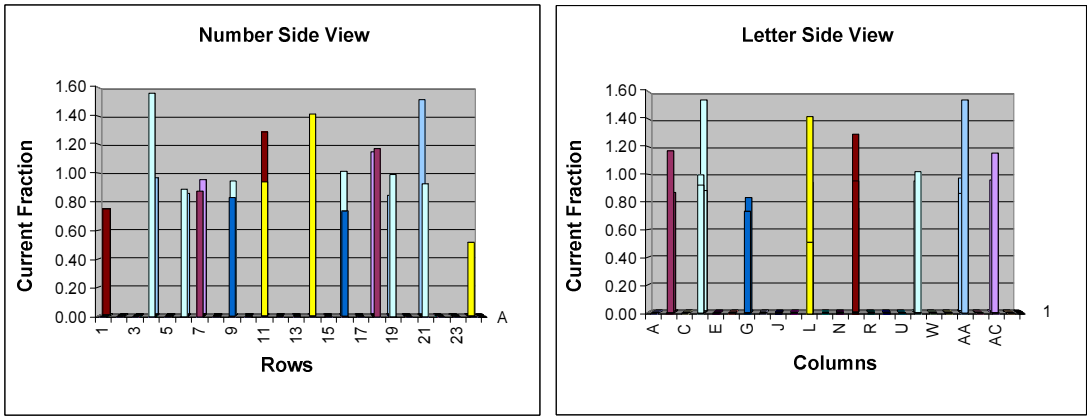


Figure 5.12 – Fractional Contributions of Bypass Capacitors

This has implications for printed circuit board design. System designers have always assumed that if bypass capacitors were relatively closely spaced, the intervening pins would current share. The measurement results contradict this assumption and indicate that the preferred path for current transients is along the *z* axis through the board to a bypass capacitor on the backside attached directly to the pin via. Certainly, capacitors do supply multiple vias, but the majority of the current will be taken by the pin to which the capacitor is directly attached.

Finally, we can use the measurement results to determine the values of $\partial I/\partial t$ that reach the printed circuit board. Figure 5.13 shows the values of rising edge $\partial I/\partial t$ for pin L11 in the central area and pin A2 at the package corner. The value of $\partial I/\partial t$ for pin A2 is 15 amperes per microsecond while the value of $\partial I/\partial t$ for pin L11 is 50% greater. This implies a variance in the values of $\partial I/\partial t$ depending on pin location. We can quantify this by measuring the maximum value of rising edge $\partial I/\partial t$ for each pin. Figure 5.14 shows the values of $\partial I/\partial t$ plotted across the chip area. There are two 3D plots: one looking from the numbered side of the package and one looking from the lettered side of the package (see Figure 5.1). The minimum value of $\partial I/\partial t$ is found to be 5 amperes per microsecond, and the maximum value is 30 amperes per microsecond at the package center. But the figure also reveals something interesting: large values (≥ 20 amperes per microsecond) are distributed all across the package area. Once again, the DUT package is reasonably efficient at spreading the current load across the package area: the central "hot spot" is not all that hot.

Recall that in Section 5.1.2 we calculated that the test sockets added 1.3 nH of inductance for adjacent VDD/VSS pin pairs. Using a $\partial I/\partial t$ value of 20 amperes per microsecond, the voltage disturbance introduced by the socket is 26 mV, or 2.6 percent of the total supply voltage of 1 volt. This is a small enough number to justify neglecting the disturbance of the sockets, but reducing this disturbance is a desirable goal for future work.

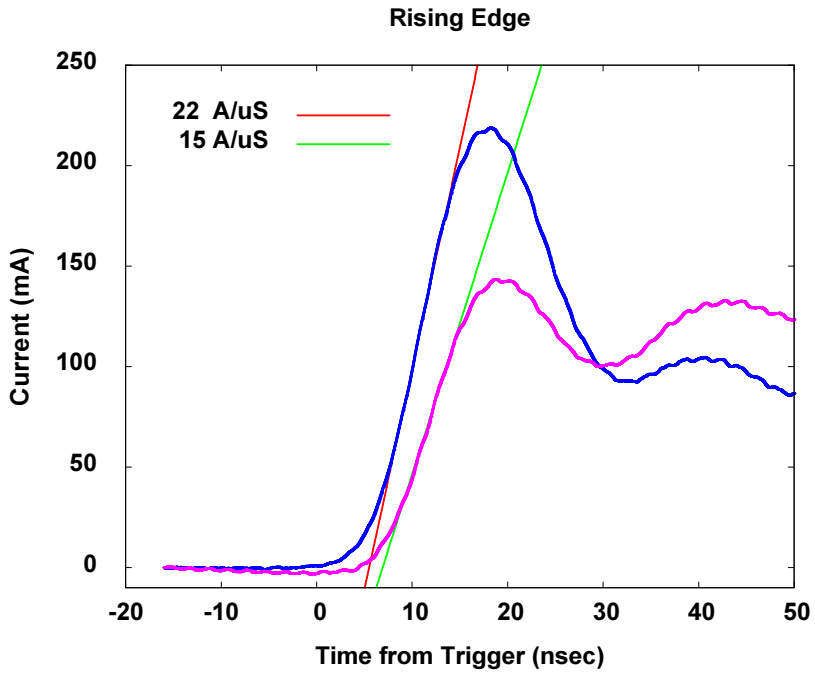


Figure 5.13 – Values of VDD Pin $\partial I/\partial t$ for Pins L11 & A2

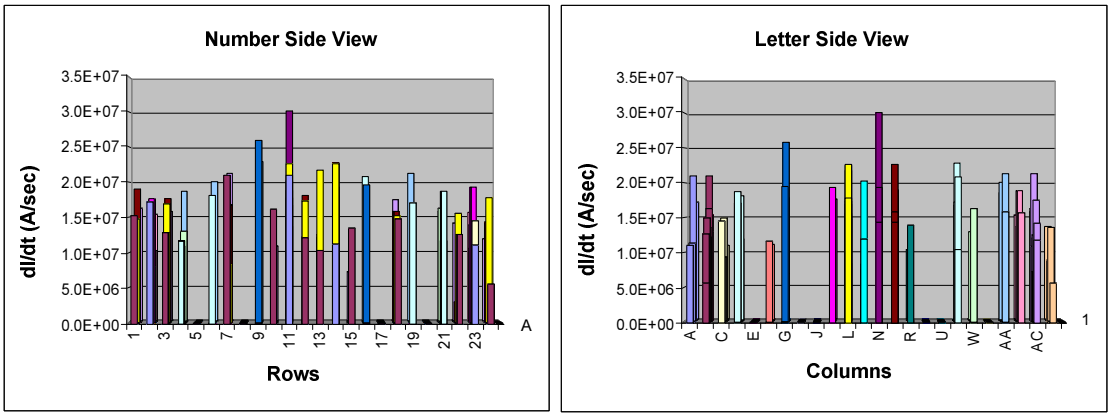


Figure 5.14 – Distribution of Values of $\partial I/\partial t$

Estimates of $\partial I/\partial t$ based on multiplying the worst case value by the number of VDD pins are sometimes used to be "conservative". But this isn't fair. First, as we've seen, the VDD pin currents exhibit a range of values of $\partial I/\partial t$. If we simply add all of the currents into an aggregate current, the maximum rate of change of this current is

$\partial I/\partial t$ = 1.2 amperes per ns, whereas multiplying the maximum value by the number of pins (89) gives a value twice this large. Second, we've seen that bypass capacitors connected to the vias of package pins are extremely effective at providing charge and thus reducing the demand on the power plane. The correct approach is to apply the distribution of current values and their rates of change to the printed circuit board in simulation. This can be done directly if the requisite modeling information is available from the IC vendor. Failing this, measurement data such as those presented here can be used to reverse engineer a model for the packaged IC which can then be applied to various printed circuit boards in simulation.

Lastly, we should confirm the validity of our assumption of quasi-static conditions. This can be done by using an FFT to obtain the power spectrum of the VDD current. Figure 5.15 shows the spectrum obtained for the aggregate VDD pin current. It is evident that the vast majority of spectral power lies below 100 MHz. There is a small amount of energy at multiples of 500 MHz, the DUT clock frequency, but the spectrum is effectively band limited at 100 MHz. In the FR4 material used for the printed circuit board, the phase shift across the package diagonal is 11% of a wavelength at 500 MHz. This confirms the validity of assuming quasi-static conditions. This result also typifies a well designed die/package/board power system. At each stage of the system, local charge storage in conjunction with equivalent series resistance or inductance forms a low pass network that filters out high frequency events. Well designed on-die and package power networks will prevent very high frequency power currents from reaching the board, and local charge storage on the board in turn prevents high frequency currents from reaching the power supplies.

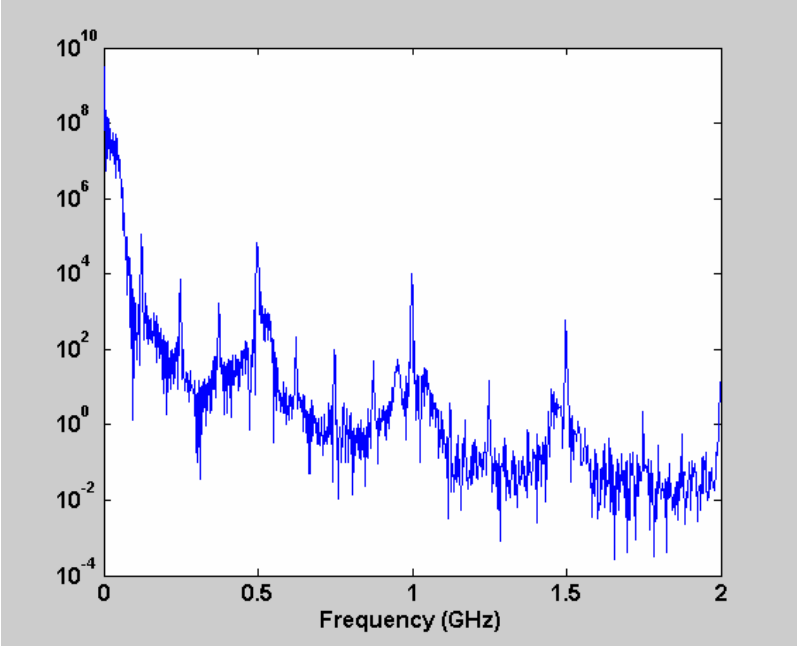


Figure 5.15 – Power Spectrum of Aggregate VDD Current

5.3 Summary

This chapter has demonstrated a method for determining the transient current as a function of time for each supply and ground package pin of ball grid array (BGA) integrated circuit packages. Using an inductive loop, the voltage induced by the transient currents is measured at each of the vias connecting the package pins to the underlying printed circuit board. Once the matrix of mutual inductances between the vias and measurement sites is known, matrix algebra and numerical integration can be used to uniquely determine each pin's current as a function of time. If, as was the case in this application, the power spectrum of the power and ground currents contains minimal energy above 500 MHz, quasi-static conditions can be assumed for packages up to 2.5 cm on a side, and the mutual inductance matrix can be easily calculated using the one-over-distance fall-off of magnetic field strength.

In the application presented, the device under test was a content addressable memory having a 1 volt core supply voltage. Using alternating sequences of consecutive matches and misses, abrupt current transitions of 8+ amperes were

created. Collectively, the current data gave some useful insights into the behavior of the power network in the underlying printed circuit board. It was seen that while the VDD and VSS current density is higher near the center of the package, three times as much total current was carried by peripheral pins. We also saw that bypass capacitors placed behind the part, on the backside of the board, are extremely effective in supplying charge. When connected directly to a pin via, these bypass capacitors supplied 80 to 120 percent of the pin's current during transients. This tight bounding indicates that there is limited current sharing to adjacent pins without attached bypass capacitors. The values of $\partial I/\partial t$ for VDD currents showed a distribution across the area of the package. The value of $\partial I/\partial t$ for the measured aggregate VDD current was half the value that would be obtained by extrapolation from the pin with the highest value, indicating the need for proper power system modeling. The measurement results could certainly be used to verify the predictions of such power system modeling. The results could also be used to generate a functional model of an integrated circuit's power current behavior if a first principles model is unavailable.

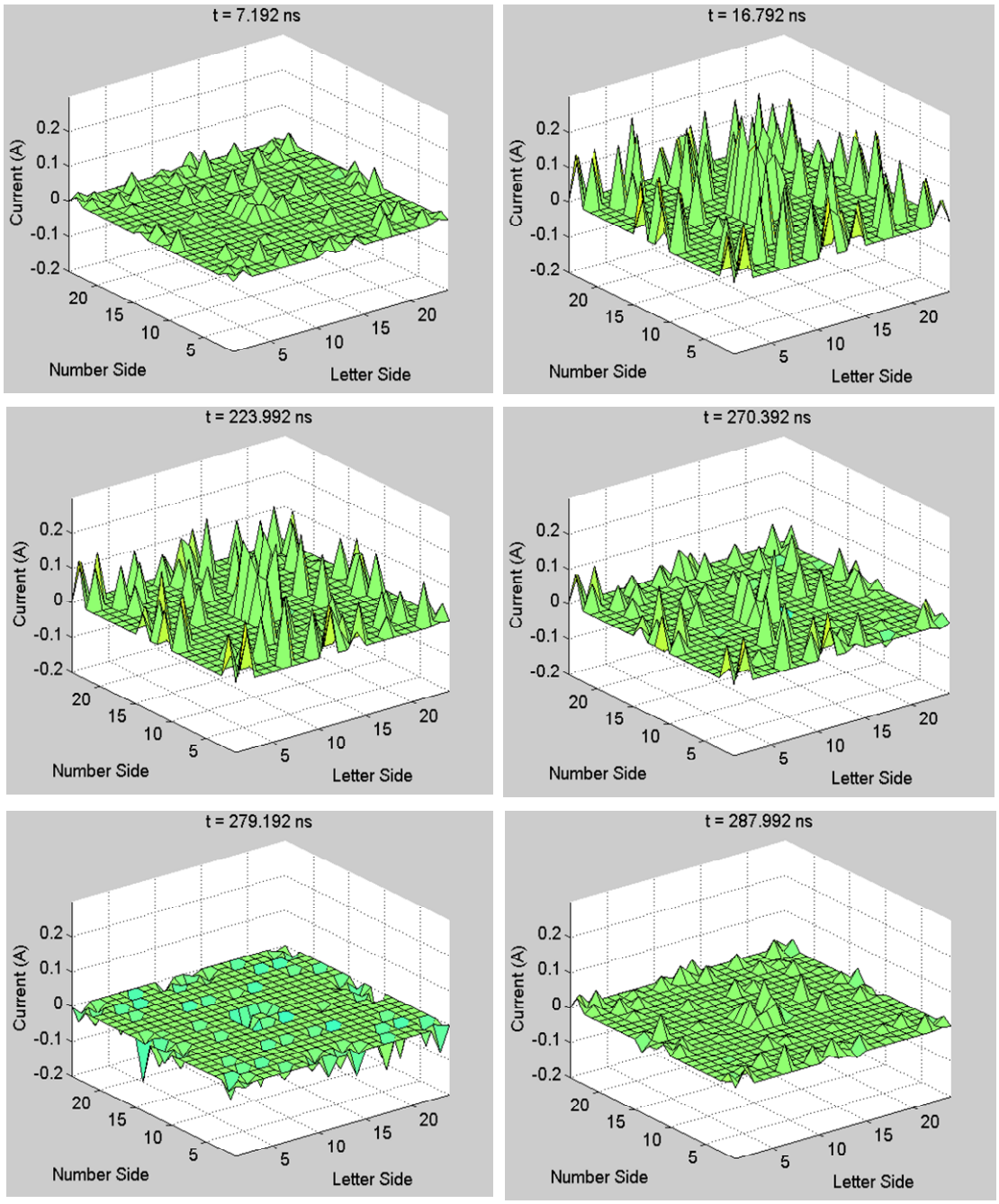


Figure 5.16 – Distribution of VDD Pin Currents
(Pin A1 is at 0,0)

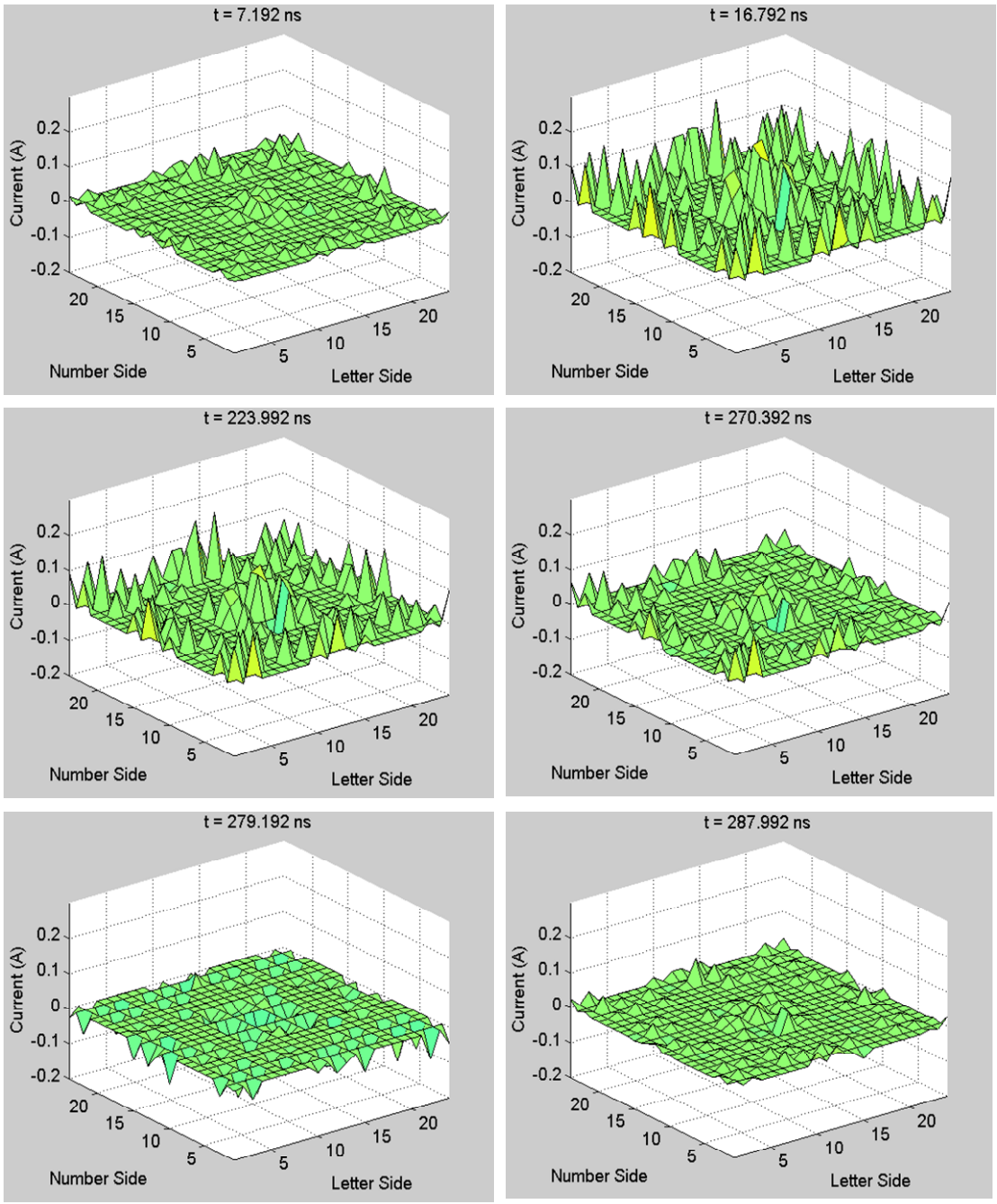


Figure 5.17 – Distribution of VSS Pin Currents
(Pin A1 is at 0,0)

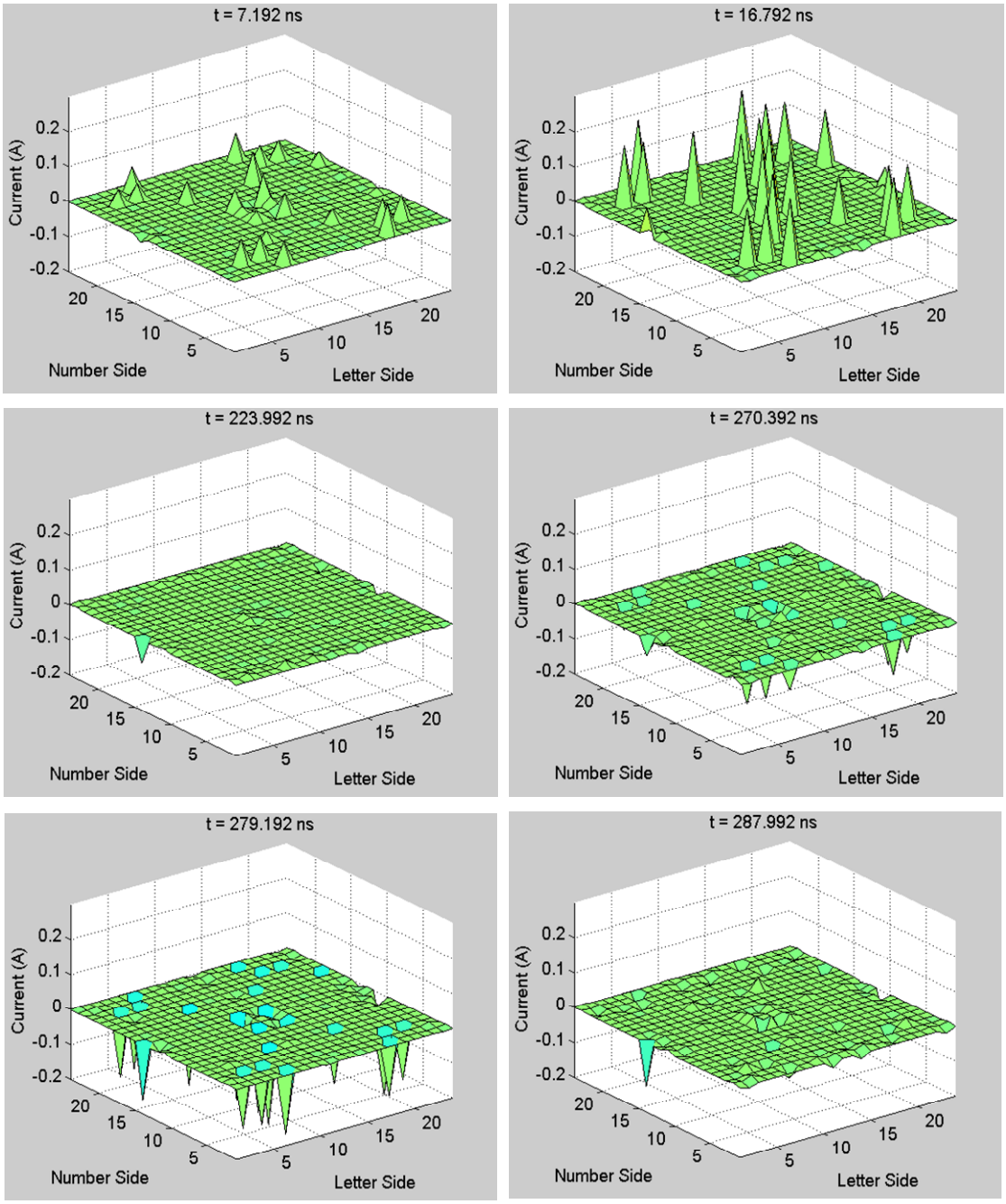


Figure 5.18 – Distribution of Bypass Capacitor Currents
(Pin A1 is at 0,0)

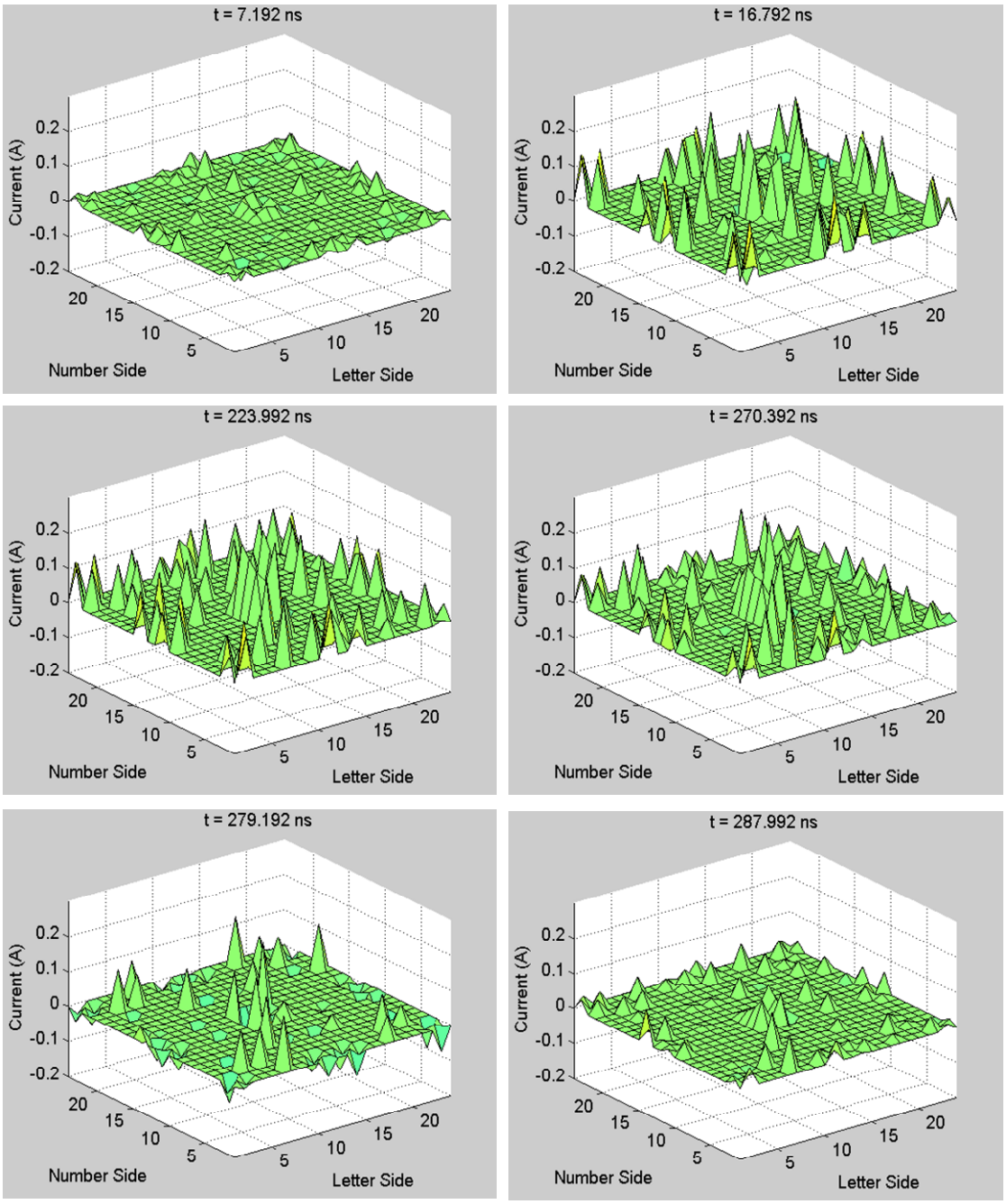


Figure 5.19 – Distribution of Power Plane Currents
(Pin A1 is at 0,0)

Chapter 6

Conclusion

This work has shown that fine-grained measurements of dynamic supply currents can be made using the magnetic fields generated by these currents. Both the design analysis of Chapter 3 and the results of the proof of concept tests discussed in Chapter 4 showed that inductive loop sensors can be inserted into industry standard printed circuit boards and have an upper frequency limit of 2 GHz. Furthermore, our supply current measurements in high performance printed circuit boards had an accuracy of about 10%. For repetitive signals, where averaging can be used, currents with a rate of change as small as 6 μA/ns can be recovered with a signal to noise ratio better than 20 dB. In Chapter 5, the method was applied to a real problem and yielded valuable data on power delivery.

Measurement of all power and ground package pin currents of a large CAM memory showed that, as system designers have long suspected, there is non-uniformity in the distribution of both the intensity and the rate of change of supply current across the IC package. The VDD current density was found to be 33% higher at the center of the package versus the package periphery. Likewise, the highest time rates of change of VDD currents were found in pins at the center of the package. The degree of asymmetry, however, was less than expected. While VDD current density was highest at the package center, three-fourths of the total current was carried by pins outside of this area, and the time rate of change of VDD current in many peripheral pins was two-thirds of the highest values at the package center. These results force the conclusion that, at least for the case studied, transient current events are spread far more evenly across the package pin area than is usually believed.

The effectiveness of bypass capacitors in supplying charge for current transients was clearly seen. During current transients lasting up to 10 ns, capacitors placed on the back of the board directly under a pin supplied 80 to 120 percent of the pin current. This was true for both pins at the center of the package and those on the periphery. Furthermore, only four out of twenty such capacitors supplied more than 120 percent of the pin's current, indicating that they were supplying neighboring pins. In contrast, capacitors placed outside the package footprint and connected to the pin by a wide, low impedance trace, supplied an average of only 50 percent the pin's current. The clear implication is that for transient current, the preferred supply path is along the *z* axis, directly through the board. Designers should not assume that bypass capacitors will effectively supply high current transients to multiple pins.

6.1 Directions for Future Work

In order to produce a practical instrument, the inductive probe should be redesigned so that it is more robust. The planar loop used is far too mechanically fragile to be practical for industrial use. Extremely precise alignment to the measurement site is required to avoid breaking the probe tip. It is also difficult to determine the exact depth of insertion. The point at which the end of the loop just enters the printed circuit board must be found by observation, and the resulting uncertainty can lead to measurement inaccuracies. Both of these problems can be solved by using a cylinder in place of a plane as the loop armature, as shown in Figure 6.1. A 450 μm diameter rod of stable, non-conductive material with a relative dielectric constant of three to four (such as a mineral filled plastic) forms the probe armature. A slot for a #40 AWG wire is laser cut down the sides and around the end of the rod, and the loop wire is cemented in the groove. The ends are attached to an SMA connector (not shown) which is secured to the rod. A chamfer on the rod end eases insertion, and a stop collar placed a known distance from the end of the rod ensures precise and repeatable depth of insertion. These improvements would also reduce the time required to make a set of measurements.

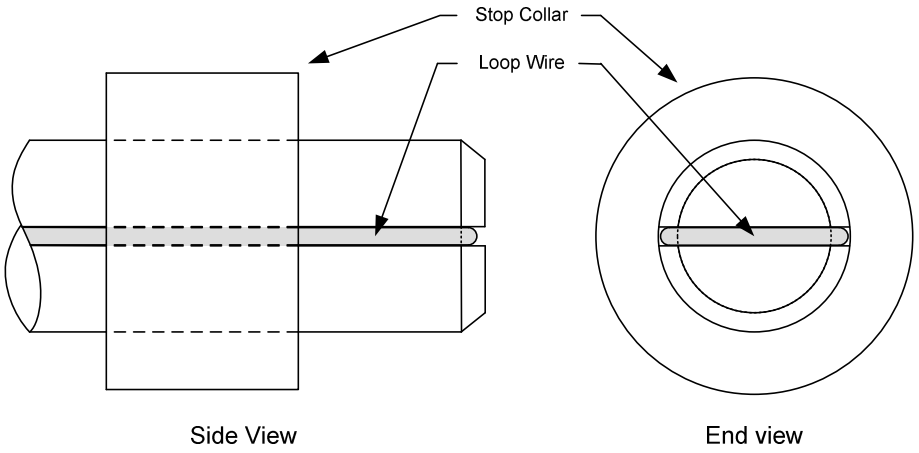


Figure 6.1 – Cylindrical Loop Armature

With these improvements, a series of correlation studies could be undertaken which compare simulations against measurements. Such studies would help to determine if the simplifying assumptions typically used are appropriate. Actually doing this, however, is complicated by the fact that simulation tools intended to be applied to the Die/package/PCB system require a fairly detailed description of the die, and IC vendors are often reluctant to disclose this information. Using the current measurement method developed in this work, vendors of integrated circuits can develop and verify models of the supply current networks of their parts. Behavioral models could then be given to system designers to enable power system design. The results discussed in Chapter 5 show that the distribution of current transients has major implications for the design of printed circuit power networks, so system designers should now require such models from IC vendors. It is possible, of course, to use this current measurement method to develop ad hoc models for packaged integrated circuits, and then use these models for printed circuit board design. But a better approach is for the IC and system design communities to collaboratively develop a sound modeling methodology which both protects intellectual property and facilitates sound overall design.

We could imagine the possibility of embedding measurement loops in test sockets and/or interposers to allow power current measurements for large integrated circuits

such as microprocessors. Also, with the on-going development of micro-vias and high density interconnect for printed circuit boards, loops might be embedded directly into the printed circuit board. It is also possible that they could be embedded in the IC package itself, provided an adequate means for connecting them to measurement circuits can be found. An array of such loops would allow the power usage of a system to be monitored dynamically. The data might then be used to control activity so as to optimize power delivery. Additionally, since this measurement approach is not limited to power system currents, such embedded loops could be useful for non-contact continuity testing. Critical signal traces between BGA packages can be difficult to access, and at-speed testing is not possible with standard "bed of nails" testers. Embedded loops would provide both signal access and at-speed measurements.

Finally, other sensor technologies might be applied to current measurement. Thin film sensors based on induction loops with ferromagnetic cores (e.g. Permalloy) would have higher inherent sensitivity, in trade for lower bandwidth, and small thickness. This might allow insertion directly under BGA packages with extended solder ball height. The printed circuit board areas around the perimeter of large packages is often obstructed by other components, so this approach is not without its problems, but it would eliminate the need for drilling the invasive non-plated hole required by the present approach. Sensors based on Hall Effect devices, giant magneto-resistance or magnetic tunnel junctions would allow sensing of DC and very low frequency (less than 1 MHz) currents. While these devices may not be able to reach 1 GHz frequencies, their use in conjunction with inductive loops would provide a DC to 2 GHz measurement range. By combining low and high frequency measurements, the total power dissipation could be measured for an individual part. This would be of great value to system designers, who usually have to rely on estimates from IC designers and global measurements covering multiple integrated circuits.

6.2 Final Thoughts

Assuring the adequacy and cost effectiveness of power delivery networks is one of the major challenges facing the designers of modern digital systems. If these networks

cannot supply sufficiently large dynamic currents, the performance of integrated circuits is compromised, and the performance potential of modern CMOS circuits cannot be achieved. A 6 GHz microprocessor is pointless if its operating frequency must be kept to 2 GHz to achieve the required supply voltage stability. Yet designers often do not have the resources to fully analyze power delivery networks. Furthermore, designers have traditionally been restricted to supply voltage and average power supply current measurements as their only diagnostic resources. This has severely restricted their insight into power network behavior. Though not glamorous, the continued development of current metrology will give designers the ability to diagnose the sources of failure in power delivery systems as well as the insight required to make these systems correct by design.

Appendix A

CAM Test Board

The test board used to make the tests described in Chapter 5 was designed to provide an electrical environment that resembled that of boards in which the CAM memory would typically be used. The PCB contained eight stripline layers, six ground plane layers for the striplines and four power/ground plane pairs. Two of these pairs were located at the center of the board, while a pair was located near the top and also the bottom of the board. The VDD/VSS plane pair for the CAM core supply was the uppermost (towards the top surface of the board) of the two power ground pairs at the board center. This placed core VDD/VSS pair approximately 20 μm off the board's center. Total board thickness was 3 mm, and FR4 dielectric was used throughout.

The completed test board is shown in top view in Figure A.1 below. To give some positional stability, the board was inserted into the chassis of a commercial Ethernet router. The chassis also supplied primary power to the on-board DC-DC converters, which can be seen at the center of the bottom edge of the board. The four SK0576BG2701A compression sockets, labeled U1 through U4, for placing the DUT are clearly visible. The compression lids of the sockets have been removed for visual clarity. SMA connectors mounted directly on the board allowed direct attachment to a Tektronix TDS7704B oscilloscope for monitoring the system clocks as well as the data acquisition trigger emitted by the controlling FPGA.

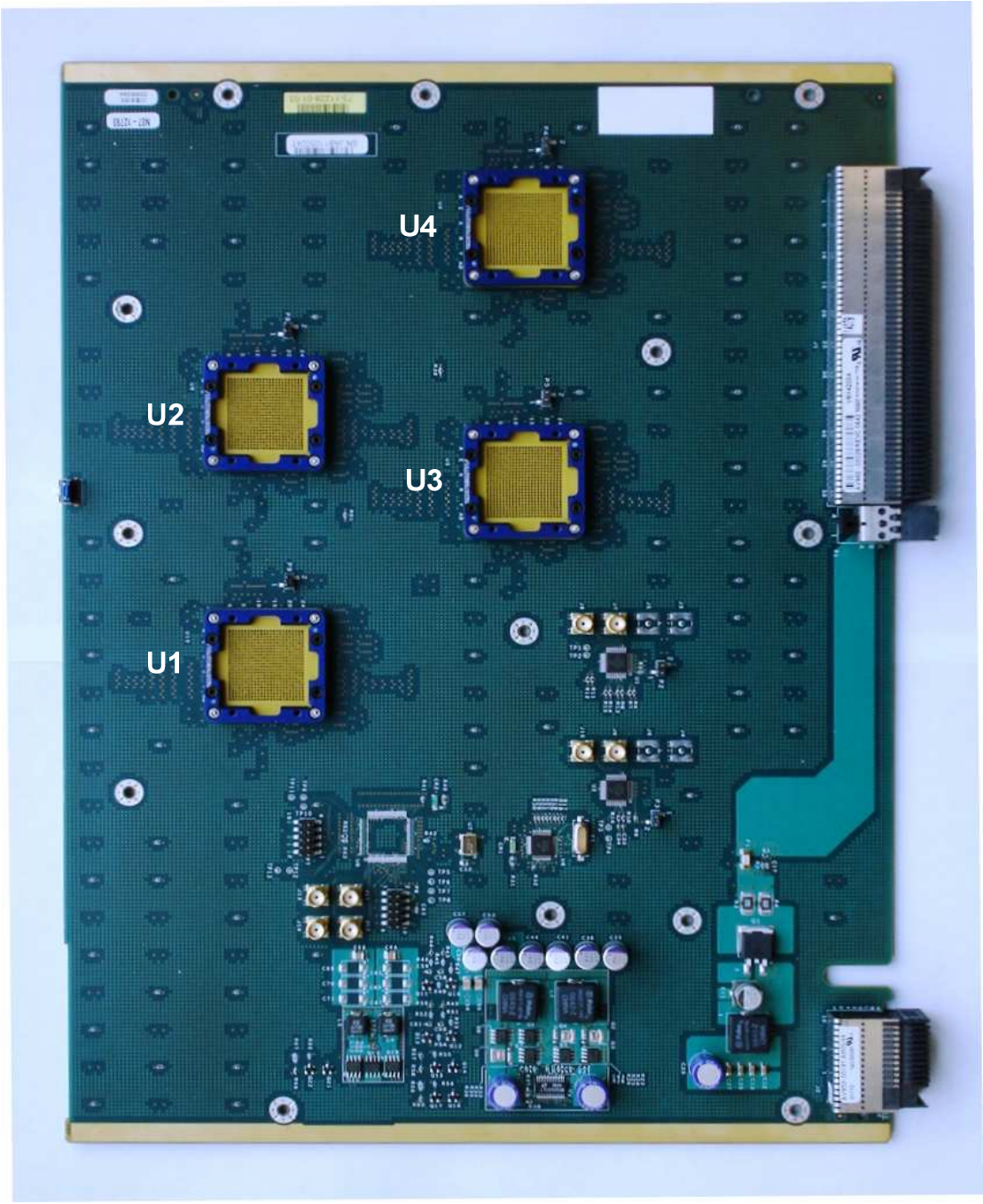


Figure A.1 – TCAM Test Board

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