# LOW JITTER CLOCKING OF CMOS ELECTRONICS USING MODE-LOCKED LASERS

A DISSERTATION

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FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

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March 2005

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To my mother

Dr. Usha Bhatnagar

# Abstract

The clock is the heart-beat of an electrical system. Most communication and processing functions in CMOS chips are triggered by a clock edge. An unstable clock can cause a system to fail or limit its frequency range of operation. Electrical clock signals are typically generated on-chip and distributed to end nodes through a symmetrical network of wires. As the number of end nodes has grown with Moore's Law scaling, the jitter and skew in electrical clock distribution have become a bottleneck to the speed of CMOS chips. Optical clocking is a radical approach in which a laser is used as the precision time source and optical distribution schemes are used instead of wire networks.

This dissertation investigates the feasibility and potential advantages of optical clocking. First, a comparative model is developed to assess the benefits and realm of applications for optical clocking in electrical systems. Next, experiments investigating the feasibility of injecting optical clocks into CMOS digital circuits are presented. Optical clock injection with hybrid detectors as well as monolithic CMOS detectors is demonstrated in this dissertation. Finally, a small scale demonstration of optical clock distribution is presented in the context of a high speed chip-to-chip link. In this demonstration we show that optical clock injection provides sub-picosecond clock jitter, and has the potential for sub-picosecond clock phase adjustment. The optical scheme provides a 3X reduction in clock jitter over an equivalent electrical scheme in this application.

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# Table of Contents

# List of Tables

**Chapter 3**



**Chapter 5**



**Chapter 6**

# List of Illustrations

**Chapter 2**



**Chapter 3**

**Chapter 4**

**Chapter 5**

**Chapter 6**

# Chapter 1

# Introductory Remarks

This dissertation shows that direct optical clock injection using mode-locked lasers is feasible and can provide low jitter clocking in small to medium scale electrical applications. We begin this chapter by explaining the importance of clocking and outlining the problems associated with conventional electrical clocking. We then introduce optical clocking and motivate the remainder of the dissertation.

The first signal to turn on upon booting a computer is its clock. The clock signal gives the computer system its time reference. Based on this reference the first instruction is loaded from memory into the microprocessor and then subsequent instructions are loaded and executed at each clock cycle. Each chip in the system uses its clock to synchronize data for on and off chip communication. The clock frequency is an indication of how fast the computer system executes instructions, and is used as a figure of merit for semiconductor chips. For example, a 3.2 GHz Pentium refers to a microprocessor that is based on a 3.2 GHz clock.

With the clock playing such an important role, non-idealities in the clock can slow down the system or cause failure. The two most important non-idealities are jitter and skew. Jitter is the amount of uncertainty in the timing of the clock edges. It is the standard deviation in the timing of a clock edge measured over a long time. Skew is the static shift or mismatch between clocks. As an example, jitter and skew on the microprocessor and memory clocks can cause errors in the communication link between them. Clearly then it is important to minimize the jitter and skew on the clock.

The problem with distributing a low jitter, low skew clock in modern electrical systems is the frequency and distance dependent loss of wires. In electrical clock distribution a single clock signal is routed to many parts of a chip or board using wires. After an ideal 1 GHz clock is transmitted through a certain length of wire, its high frequency content becomes un-usably attenuated. The only way to transmit the clock further is to use an amplifier called a repeater. One disadvantage of using repeaters is that delay mismatch between repeaters will cause skew. Another disadvantage of repeaters is

that their delay depends on the local supply voltage so noise on the supply is converted to clock jitter by the repeater.

In a 10 GHz computer the situation would be worse. Wire loss would be higher at this frequency, so more repeaters would be needed. As more repeaters are added to the distribution, the skew and jitter would increase roughly proportionally. This is because in smaller CMOS technologies while the repeaters get faster and their skew and jitter scales down, the decrease in skew and jitter is less than the decrease in cycle time. Thus as a fraction of cycle time skew and jitter increase linearly with clock rate. Additionally, the supply noise itself tends to increase due to the larger switching currents and the inductance of the supply wires. Repeaters also consume additional power and chip area.

Optical clocking has been proposed as a radical solution to some of these problems. The optical approach originally proposed by Joseph Goodman et al. in 1984 [1] uses a laser as the clock and a diffractive optical element for the distribution. A diffractive optical element is a piece of glass that converts one laser spot to an array of distinct laser spots. These spots can then be focused to an array of on-chip photo-detectors, which form the clock injection nodes. In optical clocking there are no wires or repeaters, till at least the injection nodes. A principal advantage of this approach is that there is no frequency dependent loss. The jitter and skew of an optical distribution are the same whether the clock frequency is 100 MHz or 100 GHz.

In addition to a good distribution for high speed clocking, optics offers a low jitter clock source in the form of the mode-locked laser. Mode-locked lasers are ordinary lasers with an additional mechanism that allows emission of pulses of light at a fixed repetition rate. The jitter or timing noise in mode-locked lasers can be extremely low even at

repetition rates ranging from 10 GHz to 100 GHz. The governing principle behind the low jitter of mode-locked lasers is that the quality factor or Q of laser cavities is quite high. The Q is a function of the loss in the cavity, which is essentially independent of the laser repetition rate. Hence low jitter mode-locked lasers are practical over a wide range of repetition rates.

This dissertation shows that direct optical clock injection using mode-locked lasers is feasible and can provide low jitter clocking in small to medium scale electrical applications. The next chapter will provide background by describing the related work in electrical and optical clocking. The remainder of the dissertation has two objectives. The first objective is to quantify how much jitter, skew and power can be saved by using optical clocking. This will be done in Chapter 3 by creating and analyzing a clock distribution model for comparing optical and electrical distributions. The second objective is to show the feasibility of optical clock injection using hybrid and monolithic photo-detectors and to demonstrate the jitter savings from optical clocking in a small link application. Accordingly, Chapter 4 will present optical clocking of a digital circuit using hybrid integrated detectors. Chapter 5 will focus on the characterization and use of monolithic CMOS photo-detectors demonstrating a similar optical clock injection. Chapter 6 will demonstrate jitter savings in a small link application. Finally, Chapter 7 will summarize the contributions and conclude.

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# Chapter 2

# Introduction to Electrical and Optical Clocking

First, this chapter provides background on electrical clock generation and distribution. Then, it introduces free-space receiver-less optical clocking using mode-locked lasers, in the context of prior work on optical clocking.

## 2.1. Electrical Clock Generation and Distribution

Electrical clocks are commonly generated by electrical phase-locked-loop (PLL) circuits and distributed by symmetric trees and/or grids of metal interconnect. A PLL consists of an on-chip high frequency voltage controlled oscillator (VCO) and a feedback loop. An example is shown in Fig. 2.1. The feedback loop divides the VCO output frequency and compares it to an off-chip low frequency reference oscillator using a phase-frequency detector (PFD). The error signal from the PFD triggers a set of current sources, or charge pumps, to generate the control voltage of the VCO. In the example in Fig. 2.1, a phase difference would cause one of the current sources to be on longer, causing a net voltage change on the filter/capacitor voltage $V_{control}$, which would adjust the frequency of the ring VCO shown. In this way the VCO phase locks to the reference but runs at a multiple of the base frequency. Typically the base reference frequency ranges from kHz to 100s of MHz and can be set to a number of discrete values within that range. The VCO multiplies up the reference clock frequency and is the starting point of the on-chip distribution.

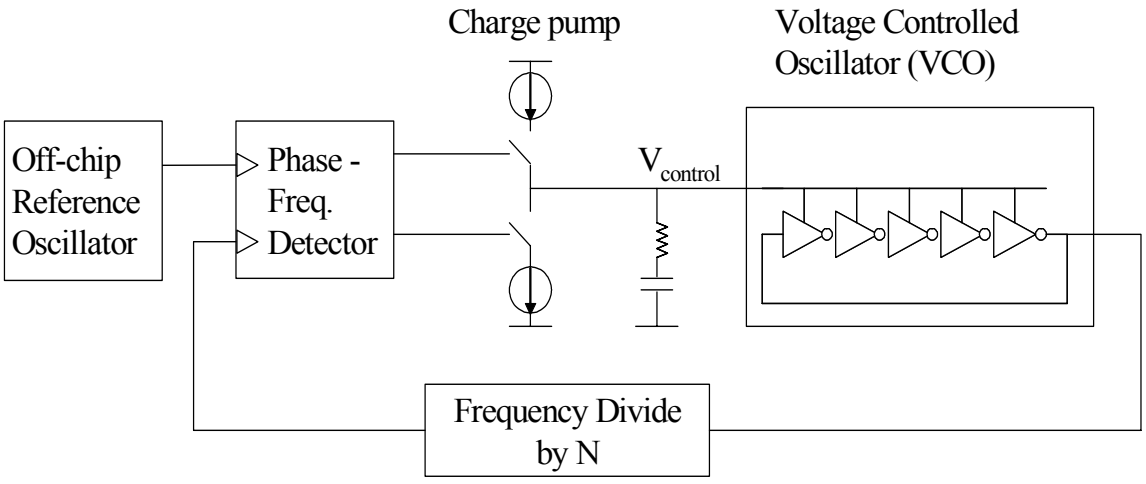
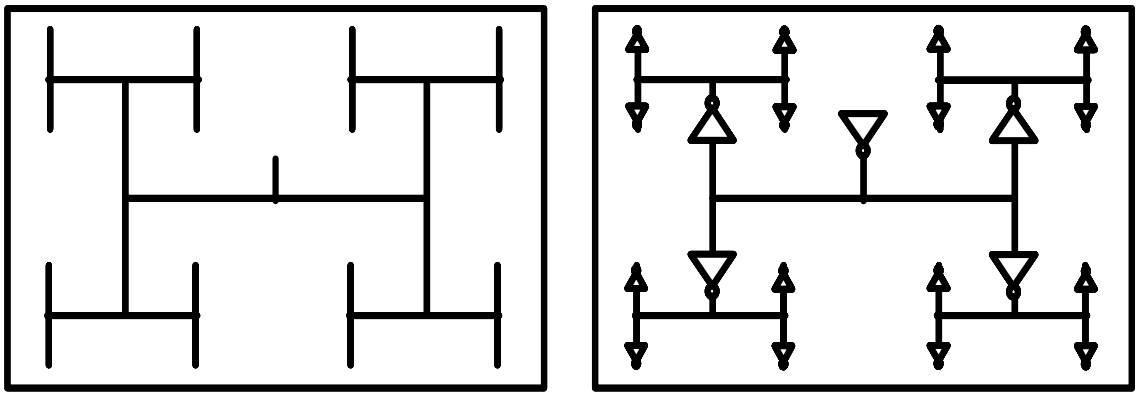



Figure 2.1 Block diagram of a Phase Locked Loop (PLL)

The quality of the delivered clock signal depends on the characteristics of the PLL and of the metal lines used to distribute the clock. Latches, flip-flops, samplers and other circuits which require the clock are spread throughout the chip. The clock is distributed to these circuits using metal lines routed in a symmetric pattern. One common pattern in which clock wires are routed is shown in Fig. 2.2 a, and is called an H-tree.

As the speed and complexity of chip designs increase, the frequency and distance dependent loss of the wires in the distribution presents challenges. Transistor scaling increases computational bandwidth by shrinking clock cycle times. To ensure proper clocking with a shorter cycle time, the rise and fall time of the clock, and the allowable variation in its arrival time, should shrink proportionally. This requires that the wires used in the clock distribution support faster transition times while introducing less variation. However, shrinking a wire in all three dimensions does not change its bit rate capacity which is determined solely by the wire aspect ratio [1]. Therefore, thicker wires are used to the extent possible. Ultimately, to scale beyond the aspect ratio limit of wires, the use of repeaters becomes necessary. Fig. 2.2 b shows an example of a modern H-tree, which consists of wires, and periodically placed repeater amplifiers.



(a) (b)

Figure 2.2 H-tree clock distribution with (a) wires only and (b) wires and repeaters

## 2.2. Figures of Merit for a Clock Distribution

Proper functionality of synchronous systems can be achieved only if the distributed clock is within tolerance on a few key figures of merit. Most important of these are jitter, skew and power consumption. Jitter is defined as the standard deviation, $\sigma_{\Delta T}$, of the time interval between the first rising edge, or trigger, and the $m^{th}$ rising edge of the clock [2]. This is shown pictorially in Fig. 2.3 (a). The jitter for *m=1* is called period jitter or cycle-cycle jitter. As *m* approaches infinity the jitter is called long-term jitter. Jitter is caused by a number of sources of random fluctuation in both the clock generation and distribution circuitry. In an open loop system the jitter gets worse as *m* increases because there is less correlation, or more random fluctuation, between the trigger and the $m^{th}$ edge. Skew can be defined as the static difference in the timing of a clock edge with respect to a reference as shown in Fig. 2.3 (b). Unintended skew is caused by process, voltage and temperature variations and device mismatch. Finally the power consumption of a clock distribution is the total electrical power needed to charge and discharge the network of wires, repeaters and end loads at each clock cycle.

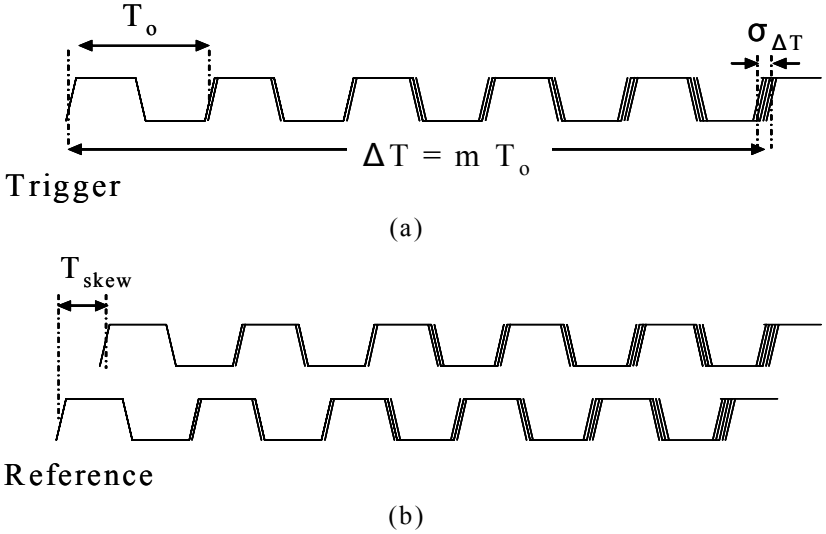



Figure 2.3 Pictorial definitions of (a) Jitter and (b) Skew

## 2.3. Problems in Scaling Electrical Clocking

The skew and jitter of the clock must remain within certain budgets to ensure error-free function of an electrical system. Specifically, the combined skew and jitter must remain less than 10 % of the clock period for most applications. Additionally, the rise/fall times are generally less than 10 % of the clock period. Thus, higher clock rates require proportionally greater absolute timing accuracy. For example, at 1 GHz the total skew and jitter must be below 100 ps, but at 10 GHz it must be below 10 ps.

As mentioned above, the wires used for distributing clocks require greater design resources with scaling because their inherent bandwidth does not keep pace. Because of the bandwidth constraint, when an ideal 1 GHz clock traverses a certain length of wire its high frequency content becomes un-usably attenuated. Fig 2.4 (a) shows that a sharp clock edge at the input of such a wire will have a much slower rise time at its output, and will need repeaters to transmit reasonably precise clock edges across a long path. Fig 2.4 (a) also shows that repeaters can potentially convert supply noise to clock jitter. Variations in the supply change the repeater delay, which translates a slow rising input to a fast rising output with jitter. Another disadvantage of repeaters is that process, voltage and temperature mismatch between repeaters in different branches of the clock tree can increase the unintended skew. Despite these drawbacks, at 1 GHz the clock distribution requires repeaters only for the global clock distribution.

Scaling such an electrical clock distribution to 10 GHz can be difficult. As shown in Fig. 2.4 (b), wire loss is higher at 10 GHz so repeaters are needed even for shorter wires and the long global clock wires require more repeaters per wire. Additionally the supply

noise might increase with scaling[1]. The total jitter and skew would increase as the number of repeaters grows.

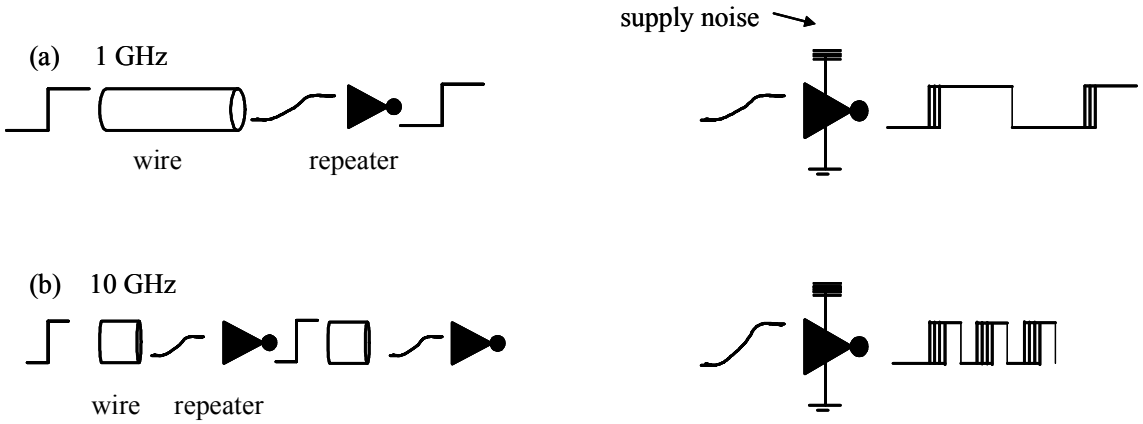



Figure 2.4 The effect of repeaters on wires at (a) 1 GHz and (b) 10 GHz

Another way to view the problem in scaling electrical clock distribution is to consider that the latency, expressed in number of clock cycles from the top of the clock tree to the end nodes, increases with scaling. This is simply because the cycle time shrinks whereas the size of the clock domain remains constant or grows. Jitter increases with latency as was shown in Fig. 2.3, because a greater number of random fluctuations accumulate over time. Skew also increases with latency. Qualitatively, as the path from the clock source to the clocked node gets longer, the factors causing the jitter and skew, such as the number of repeaters, increase. If the noise sources are strictly uncorrelated the accumulated noise increases in proportion to the square root of the latency [3, 4]; for correlated noise, however, the increase is linear.

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[1] Power supply noise is the result of LdI/dt fluctuations and coupling from nearby circuits to the supply and the substrate. The total current drawn from the supply has been increasing while the switching time and the supply voltage itself have been decreasing, so the supply noise from LdI/dt and coupling increases with scaling.

Aside from the distribution, the clock generation PLLs can also contribute to clock jitter. Perhaps most important is the effect of power supply noise since the PLL often operates in a noisy digital environment. Innovative oscillator circuits with high supply noise immunity have been designed and are continually improved [5, 6]. The thermal noise, flicker noise and 1/f noise of the devices in the PLL are relatively small, but may become important as oscillator jitter targets shrink to < 1 ps.

In summary, increasing delay (measured in clock cycles) in the clock distribution combined with an increasing use of repeaters leads to increased jitter and skew at higher frequency, whereas the requirement is for these metrics to remain a constant proportion of the clock cycle time. The number of repeaters required continues to increase with clock frequency, as does the clock jitter and power consumption. These trends make clock distribution and clock integrity a serious challenge in electrical systems today and even a greater challenge at 10 GHz and beyond.

## 2.4. Optical Clock Distribution Background

Light is an ideal carrier for high speed signal propagation. Optics replaced electrical wires decades ago for long haul communications because the distance dependent loss and low bandwidth of wires limited their capacity. Similar needs have led to the introduction of optics at progressively shorter length scales, for communication between systems and potentially between chips. With the possibility of light coming down to CMOS chips, the idea of using light to enhance the timing accuracy of high speed electrical circuits becomes relevant.

Optical clock distribution, which uses a laser as the clock source, was first proposed in a seminal paper by J. W. Goodman et. al. in 1984 [7]. The primary motivation for optical

clocking then was to minimize global clock skew. It was assumed that optical signals would be distributed at a high level on a chip or board with the lower levels of distribution done electrically. Experimental research efforts since then have concentrated on two different approaches to the distribution of light beams. The 'guided wave' distribution approach is so called because the light paths are defined by waveguides, which can be fibers or integrated on-chip waveguides. In contrast, the 'free-space' approach is based on the diffraction of light from an element similar to a grating to obtain an array of beams from a single beam and to image these onto the clock nodes.

Guided wave clock distribution relies on fibers or integrated on-chip waveguides. In 1991 Delfyett [8] demonstrated the distribution of a 302 MHz optical clock from a mode-locked laser to 1024 ports via multimode optical fiber. A fiber based distribution is unsuitable at the chip level but could be useful at the board or system levels [9, 10]. The primary concerns with this distribution are fiber to detector alignment, and uniformity. Guided wave chip-scale clock distribution requires waveguides fabricated on chip, preferably with CMOS compatible fabrication methods [11]. Coupling losses into and out of the integrated waveguides are the major drawback while propagation and bending losses are also significant. The integrated approach is also inflexible once fabricated.

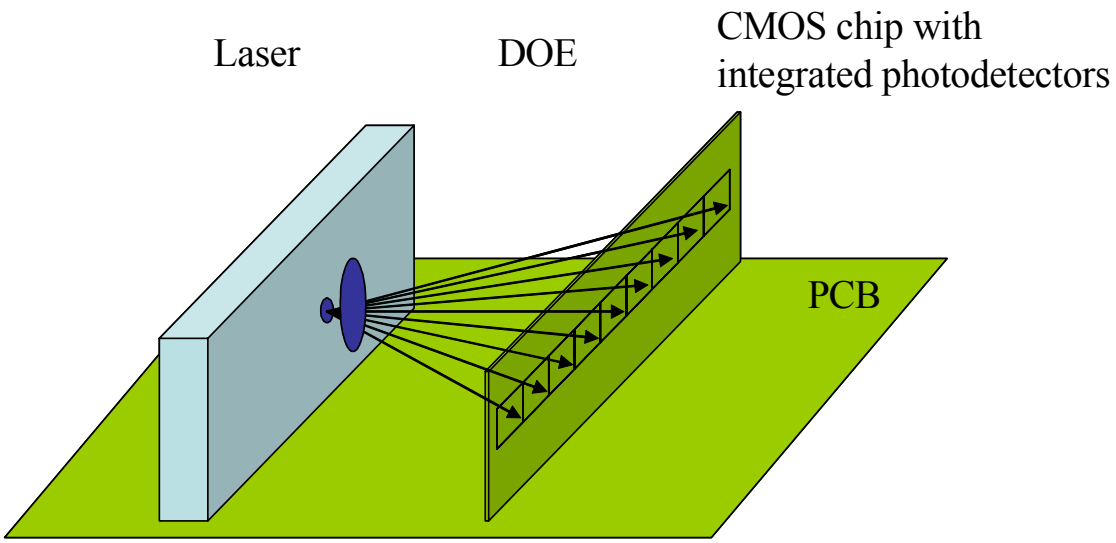


Figure 2.5 Free-space optical clock distribution uses a diffractive optical element (DOE) to generate an array of beams from a single laser and focus them onto individual photo-detectors integrated on a CMOS chip

In free-space optical clock distribution light beams propagate in air and through a diffractive optical element (DOE) to achieve the distribution. Free space distributions are viable at much shorter length scales ranging from a few mm to ~ 1 m for on-chip or chip-to-chip distribution. A DOE can be a piece of glass with a computer generated hologram etched into it. The hologram can act as a grating and lens to generate a pattern of focused spots at the detectors as shown in Fig 2.5. One advantage of the free-space approach is simplicity, because a single optical element takes the place of a network of waveguides or wires. The need to route a high-speed signal, electrical or optical across the surface of the chip is eliminated. Another advantage is that optical signals traveling in free space do not incur propagation loss or distortion. The efficiency of this scheme can therefore be as high as 80 % with less than 5 % spot intensity variation [12]. This dissertation is limited to free-space optical clock distribution because of its simplicity, efficiency and promise for chip-scale application.

Finally, recall that the major problem in electrical clock distribution is the inability to scale the distribution to high speeds without compromising jitter, skew and power consumption. A key feature of optical clock distribution is that the jitter and skew are independent of the clock rate. The jitter and skew in optical distribution is the same whether the clock is 100 MHz or 100 GHz.

## 2.5. Receiver-less Optical Clocking with Mode-Locked Lasers

For applications requiring an extremely stable high frequency oscillator, optics offers a solution in the form of the mode-locked laser. Mode-locking is a mechanism unique to optics, whereby a laser can be made to emit light in a train of short pulses. The duration of these pulses can be as short as femtoseconds ($10^{-15}$s) while the repetition rate can range from MHz to hundreds of GHz. The repetition rate of the pulses from a mode-locked laser is solely determined by the round-trip time in the laser. Since the light in a laser cavity effectively makes several round trips prior to emission, the quality factor or Q of a mode-locked laser is quite high, making the generated pulse stream a very stable clock source. Because losses in optical cavities have little dependence on frequency, it is relatively straightforward to make high-Q optical resonators, in the 10's or even 100's of GHz range of repetition rates. The primary sources of jitter are spontaneous emission and mechanical fluctuations of the cavity length [13]. Hence, fundamentally, a mode-locked laser producing sub picosecond pulses with gigahertz repetition rates can have jitter on the order of a few hundred femtoseconds or less [14].

Jitter is a potentially difficult challenge for electrical clocking at high speeds, as discussed in section 2.3 above. To benefit from the low timing jitter and fast rising edges of mode-locked laser pulses it may be best to introduce as little circuitry between the

photo-detector and the clocked node as possible. Therefore this work has proposed the use of a receiver-less detection scheme. The receiver-less ideal is to drive the input capacitance of a clocked element directly with the photocurrent from the detector, without an intervening receiver circuit. This eliminates the power, jitter and latency of the clock receiver, thereby addressing key clocking challenges.

This dissertation comprises the first demonstrations of the use of a mode-locked pulse train to deliver full-swing square wave clocks to CMOS chips with picosecond precision using integrated photo-detectors which directly drive the clock load. Fig. 2.6 shows how this is achieved. The light from the mode-locked laser is split into two beams using a beam splitter and one of those beams is delayed by T/2 where T is the laser repetition rate. The two beams are then separately focused onto two on-chip photo-detectors which are connected in series as shown. When a pulse arrives at the top detector, a photocurrent is produced which raises $V_x$ up to ~ VDD. Similarly after time T/2, the bottom detector receives a pulse which resets $V_x$ to ~ ground. Thus, the alternating pulses inject a precise square wave clock onto the chip, where a load can be driven either directly or after a buffer for capacitive gain.

Since there is no receiver amplifier, the characteristics of the photo-detectors determine the speed and required optical power for this technique. The clock rise and fall times are given by the carrier transit times in the photo-detector. To minimize the optical power the detector capacitance must be minimized. The detectors also limit the swing of the node in the middle. Since the voltage over a detector diode cannot rise above the built-in voltage in forward bias, the voltage at the middle node can rise above VDD or fall below ground by up to the built-in voltage of the diode. The silicon footprint required

for receiver-less detectors is a very small fraction of the chip area as will be shown in Chapter 3. More importantly, Chapter 3 will quantify the latency and power savings of receiver-less optical clock distribution relative to conventional electrical distribution.

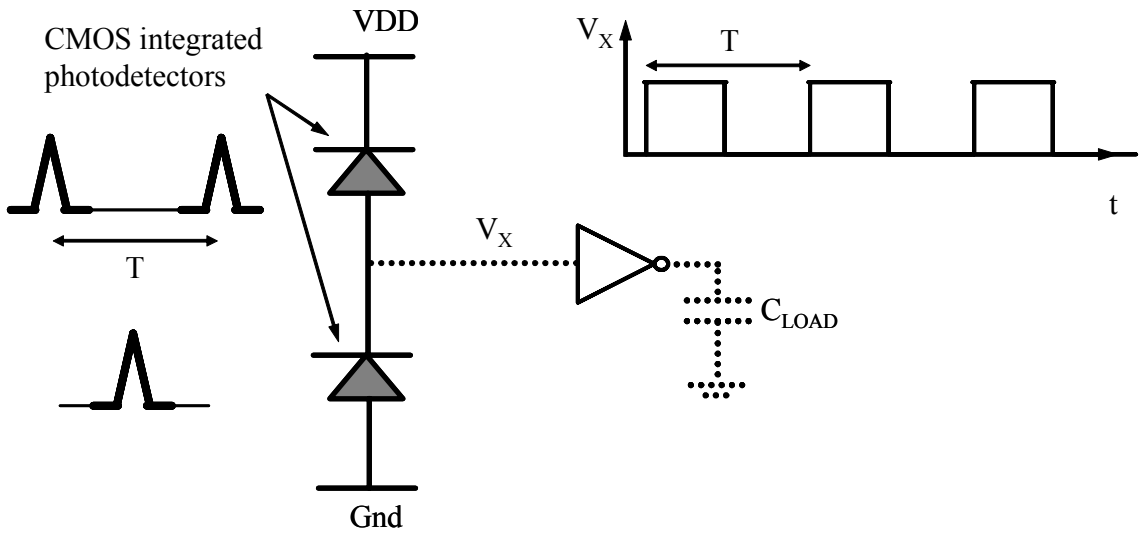


Figure 2.6 Full-swing optical clock injection using mode-locked laser pulses and receiver-less detection

The receiver-less approach also has other potential advantages. If the photo-detectors are fast, the injected clock can have a slew-rate sharper than the edges that can be created by the transistors on chip. The creation of these very sharp edges can provide noise immunity and can also be exploited on-chip to trigger specific circuits, such as samplers. These optically triggered samplers can lead to more accurate measurements of time-critical signals on chip. Chapters 4 and 5 will investigate the integration and design of photo-detectors. Another potential advantage is that the delay of the impinging short pulse stream can be adjusted with femtosecond accuracy by changing the optical path length (e.g., in the laboratory, using the combination of a translation stage and a corner-cube reflector in the optical path). Hence, it is possible to adjust clock duty cycle and to

generate accurate multiphase clocks for high speed multiplexing or de-multiplexing circuits. Chapter 6 will use this idea for a link application and Chapter 7 will conclude.

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# Chapter 3

# Optical vs. Electrical Clock Distribution:

# A Quantitative Comparison

In this chapter, a model for electrical clock distribution will be developed and used to compare the merits of optical clock distribution versus conventional electrical clock distribution. The goal of the chapter is to quantify how much benefit optical clocking could provide specifically in jitter, skew and power consumption. The dependence of these metrics in the optical case on total laser power, detector capacitance and semiconductor chip scaling will also be discussed.

## 3.1. A Model for Electrical Clock Distribution

Optical clock distribution has been the subject of research interest for two decades as discussed in Chapter 2. A quantitative analysis is necessary to understand the tradeoffs involved in optical clocking and to suggest what type of electrical applications could benefit from such a technology and to what degree. To answer these questions, first consider the electrical clock distribution of a modern semiconductor chip. Progressively replacing parts of this model with an optical distribution gives quantitative results for the savings and tradeoffs involved.

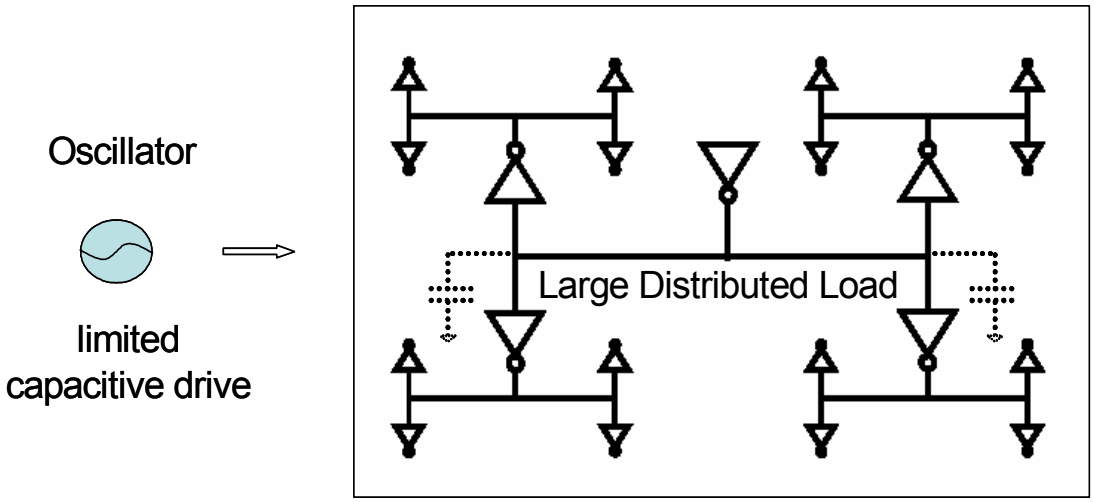


Figure 3.1 Electrical oscillator driving H-tree clock distribution with wires and repeaters

The task in electrical clocking is to take the output of an oscillator which has limited capacitive drive and use it to clock a large distributed load capacitance. In modern microprocessors a symmetrical configuration of wires and repeaters is used to achieve this [1]. One common symmetrical configuration is an H-tree, shown conceptually in Fig. 3.1. The wires and repeaters in an electrical distribution add an overhead in terms of capacitive load and clock delay or latency. The added capacitance represents the

overhead in power consumption due to the distribution. The added latency is equal to the total RC delay of the wires and any delay in the repeaters. Typically, the jitter and skew in the distribution is proportional to this latency. An optical distribution can remove some fraction of this overhead to provide the resulting savings in latency and power consumption.

This chapter will describe a working model of electrical clock distribution that has the same high level characteristics as real-world microprocessor distributions, such as those published in the literature[2-4]. A geometrically symmetric H-tree that has a capacitive and physical fan-out of 4 at each successive level will be used. The wire and repeater characteristics will be based on known parameters for a given CMOS technology. The basic assumptions of the model are listed below and illustrated in Fig. 3.2 which shows the top four repeater levels of the H-tree model.

### 3.1.1. Basic Assumptions of Clock Distribution Model

- The model is geometrically symmetric i.e.
  - the chip is assumed to be a square of length L on a side
  - the three top level wires ( k = 1 ) are each L/2 in length, and the wires at each subsequent level are shorter by a factor of two[1] i.e. L/4 ( k = 2 ), L/8 ( k = 3 ) …
  - each repeater drives four repeaters at the next level and the intervening wires
- Each repeater drives a load equal to four times its input capacitance. Such a fan-out-of-four (FO-4) configuration generally results in a close-to-minimum delay [5]. As a

[1] Note that even though these top most level wires may be considered quite long from a delay perspective, the resistance of all wires is chosen such that overall wire delay in the model is less than one third of the total clock delay.

consequence, the driving repeater at each level is slightly larger than that at the next level since it has to drive not only four repeaters but also the intervening wire capacitance. (Note that if wire capacitance were negligible, all repeaters would be the same size).

- It is assumed that the tree is driven at the very top by an active time alignment circuit such as a PLL which has limited capacitive drive. Since the repeaters in the distribution get larger towards the top, the PLL output is buffered up to drive the top level repeater. These extra buffers at the top are again a FO-4 chain, and are shown schematically in Fig 3.2.
- The distribution ends at the nth level repeater. The wires and latches that follow form $C_{load}$.

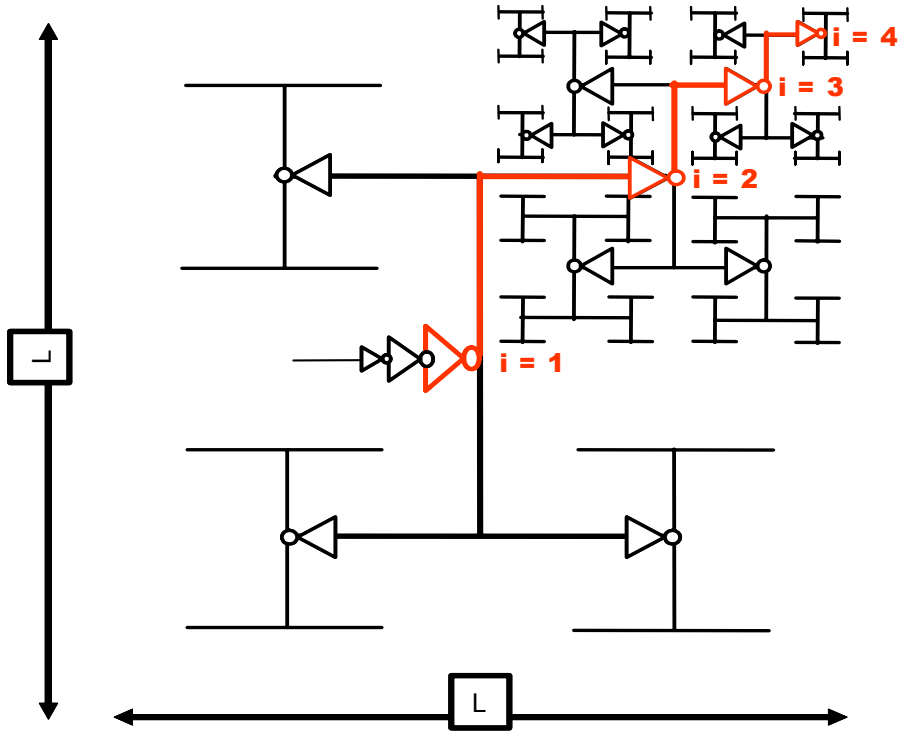


Figure 3.2 Geometrical H-tree model of electrical clock distribution

### 3.1.2. Calculation of Tree Delay and Power Consumption

The clock delay to the $k^{th}$ level repeater in the tree can be calculated by summing up the delay along a path from the PLL to one of the $k^{th}$ level repeaters. Such a path is shown in red in Fig. 3.2. To calculate this, consider that the delay between level *i* and *i+1* is equal to one repeater delay or $t_{FO4}$, plus the *RC* delay of the wire to the next repeater, i.e.:

$$t_{delay,i} = t_{FO4} + \frac{1}{2} C_W R_W l_i^2 \tag{3.1}$$

where, $R_W$ and $C_W$ are the wire resistance and capacitance per unit length. Since the model assumes that the wires at the top level have length L/2 and that they get shorter by a factor of two at each subsequent level, $l_i = L/2^i$. The total wire delay to a level *k* repeater is the sum of equation (3.1) over the top *k-1* levels, plus an additional delay due to the initial PLL capacitive drive buffer whose length, BL, will be calculated below. Thus, the total delay along one path of the conventional electrical distribution tree is:

$$\begin{aligned} t_{delay,Electrical} &= t_{FO4} \cdot k + \frac{C_W R_W L^2}{2} \sum_{i=1}^{k-1} \left( \frac{1}{4^i} \right) + t_{FO4} \cdot BL \\ &= t_{FO4} \cdot k + \frac{C_W R_W L^2}{6} \left( 1 - \frac{1}{4^{k-1}} \right) + t_{FO4} \cdot BL \end{aligned} \tag{3.2}$$

The power consumption of the clock distribution is determined by the energy needed to charge and discharge all the capacitance in the tree every clock cycle. To calculate the total capacitance in the tree, consider that a repeater at the $i^{th}$ level, with input capacitance $C_{in,i}$ drives the capacitance of three wires of length $l_i$ and four repeaters each with input capacitance $C_{in,i+1}$. Since each repeater drives four times its input capacitance the following recursive equation and its simplification apply:

$$C_{in,i} = \frac{1}{4}\left[ C_W \cdot \frac{3L}{2^i} + 4 \cdot C_{in,i+1} \right]; \quad C_{in,n} = C_{in}$$
$$C_{in,i} = C_{in} + \frac{3L}{2} C_W \left( \frac{1}{2^i} - \frac{1}{2^n} \right) \tag{3.3}$$

where $n$ is the total number of levels in the tree and $C_{in}$ denotes the input capacitance of a repeater at the last or $n^{\text{th}}$ level. Note that the last level repeaters are the smallest repeaters in the tree. In contrast, the first level repeater can be too large to drive directly with a PLL so an additional buffer chain will be required at the top. Under the simplifying assumption that the PLL drive strength is equal to $C_{in}$, the length of the buffer chain is:

$$BL = \log_4 \left( \frac{C_{in,1}}{C_{in}} \right) = \log_4 \left[ 1 + \frac{3}{2} \frac{C_W L}{C_{in}} \left( \frac{1}{2} - \frac{1}{2^n} \right) \right]$$
$$\approx \log_4 \left( \frac{3}{4} \frac{C_W L}{C_{in}} \right) \quad (\text{for } 2^n >> 1 \wedge C_W L >> C_{in}) \tag{3.4}$$

The simplification in the above equation assumed a large distribution network ($2^n >> 1$) and a global wire capacitance, $C_W \cdot L$ that is significantly larger than the last level repeater capacitance $C_{in}$. Both of these assumptions are reasonable for microprocessors. The total capacitance in the tree can now be calculated. Using equation (3.3) the capacitance of all the repeaters till level $k$ in an $n$ level tree is:

$$C_{totInv,k} = \sum_{i=1}^{k} 4^{i-1} C_{in,i} = \left( \frac{C_{in}}{3} - \frac{C_W L}{2^{n+1}} \right) \left( 4^k - 1 \right) + \frac{3 C_W L}{4} \left( 2^k - 1 \right) \tag{3.5}$$

Similarly the total wire capacitance till the $k^{\text{th}}$ level repeater in an $n$ level tree is calculated below. Note that the wires after the last repeater level along with the latches they connect to are assumed to be part of the clock load, and thus not a part of the distribution itself.

$$C_{totW,k} = \sum_{i=1}^{k-1} \frac{3L}{4} 2^i C_W = \frac{3}{2} C_W L \left(2^{k-1} - 1\right) \tag{3.6}$$

Finally, to account for the capacitance in the buffer at the top of the distribution tree:

$$C_{Buf} = \sum_{i=0}^{BL-1} C_{in} 4^i = C_{in} \frac{4^{\log_4\left(\frac{3}{4}\frac{C_W L}{C_{in}}\right)} - 1}{3} \approx \frac{C_W L}{4} - \frac{C_{in}}{3} \tag{3.7}$$

Note that the buffer capacitance is quite small and nearly independent of the size of the distribution tree *n*. Therefore the power consumption of the top buffer, equation (3.7) can be neglected relative to equations (3.5) and (3.6).

The total capacitance of the distribution network, which is directly proportional to its electrical power consumption, is the sum of equations (3.5), (3.6) and (3.7):

$$\begin{aligned} C_{tot,Electrical} &= C_{totInv,n} + C_{totW,n} + C_{Buff} \\ &= C_{in} \frac{(4^n - 2)}{3} + C_W L \cdot 2^n - 2 C_W L \left(1 - \frac{1}{2^{n+1}}\right) \end{aligned} \tag{3.8}$$

Substituting the PLL buffer length BL from equation (3.4) into equation (3.2), the total delay of the clock tree can be rewritten as:

$$\begin{aligned} t_{delay,Electrical} &= t_{FO4} \cdot n + \frac{C_W R_W L^2}{6} \left(1 - \frac{1}{4^{n-1}}\right) + t_{FO4} \cdot BL \\ &\approx t_{FO4} \left(n + \log_4 \frac{3 C_W L}{4 C_{in}}\right) + \frac{C_W R_W L^2}{6} \end{aligned} \tag{3.9}$$

Equations (3.8) and (3.9) form the basis of the electrical clock distribution model to which optical distribution will be compared. Finally, note that the key unknown parameter in these equations is the input capacitance of each $n^{th}$ stage repeater. There are $4^{n-1}$ $n^{th}$ stage repeaters and each one drives four times its input capacitance. These

repeaters drive the wires and latches that comprise the load, therefore $C_{in}$ is related to $C_{Load}$, the total latch and last level wiring load as:

$$n = \log_4 \frac{C_{load}}{C_{in}} \quad \Rightarrow \quad C_{in} = C_{load} / 4^n \tag{3.10}$$

## 3.2. Quantifying the Potential of Optical Clocking

The clock distribution model developed above is the starting point for a quantitative comparison of optical and electrical clock distribution. In an optical distribution the oscillator is a laser with limited optical output power. It drives a certain number of photo-detectors injecting an optical clock to some number of points on a chip. Consider an optical clock distribution where the wiring and repeaters up to the $k^{\text{th}}$ level repeater have been removed and replaced by an optical clock distribution comprising a central laser and on-chip photo-detectors. The light from the laser may be routed and focused onto the photo-detectors using a diffractive optical element as discussed in Chapter 2. Fig. 3.3 shows a schematic where the top two levels, shown in red, have been removed and replaced by receiver-less photo-detectors shown in blue. For the purposes of this analysis, the photo-detectors maybe connected as a totem pole at each injection point or may be single ended; only $C_{Det}$, the photo-detector capacitance per injection point, and $t_{Det}$, the rise and fall time delay of the photo-detector are relevant.

Based on equations (3.5) – (3.8) the total capacitance of the tree with optical injection to the $k^{\text{th}}$ level is:

$$
\begin{aligned}
C_{Optical,k} &= C_{totInv,n} + C_{totW,n} - C_{totInv,k} - C_{totW,k} + 4^{k-1} C_{Det} \\
&= C_{tot,Electrical} - \left( \frac{C_{in}}{3} - \frac{C_W L}{2^{n+1}} \right) \left( 4^k - 1 \right) - \frac{3 C_W L}{4} \left( 2^k - 1 \right) - \frac{3}{2} C_W L \left( 2^{k-1} - 1 \right) + 4^{k-1} C_{Det} \\
&\approx C_{tot,Electrical} - \left( \frac{C_{in}}{3} \right) \left( 4^k - 1 \right) - \frac{C_W L}{2} 2^k \left( 3 - \frac{1}{2^{n-k}} \right) + 4^{k-1} C_{Det}
\end{aligned}
\qquad \textbf{(3.11)}
$$

Dividing this by $C_{tot,Electrical}$ gives the ratio of electrical power consumed in a tree with optical insertion to the $k^{th}$ level versus an all-electrical tree, i.e.

$$
\frac{P_{Optical,k}}{P_{Electrical}} = 1 - \frac{C_{in}}{3 C_{tot,Electrical}} \cdot \left( 4^k - 1 \right) - \frac{C_W L}{2 C_{tot,Electrical}} \left( 3 - \frac{1}{2^{n-k}} \right) \cdot 2^k + \frac{C_{Det}}{C_{tot,Electrical}} \cdot 4^{k-1} \qquad \textbf{(3.12)}
$$

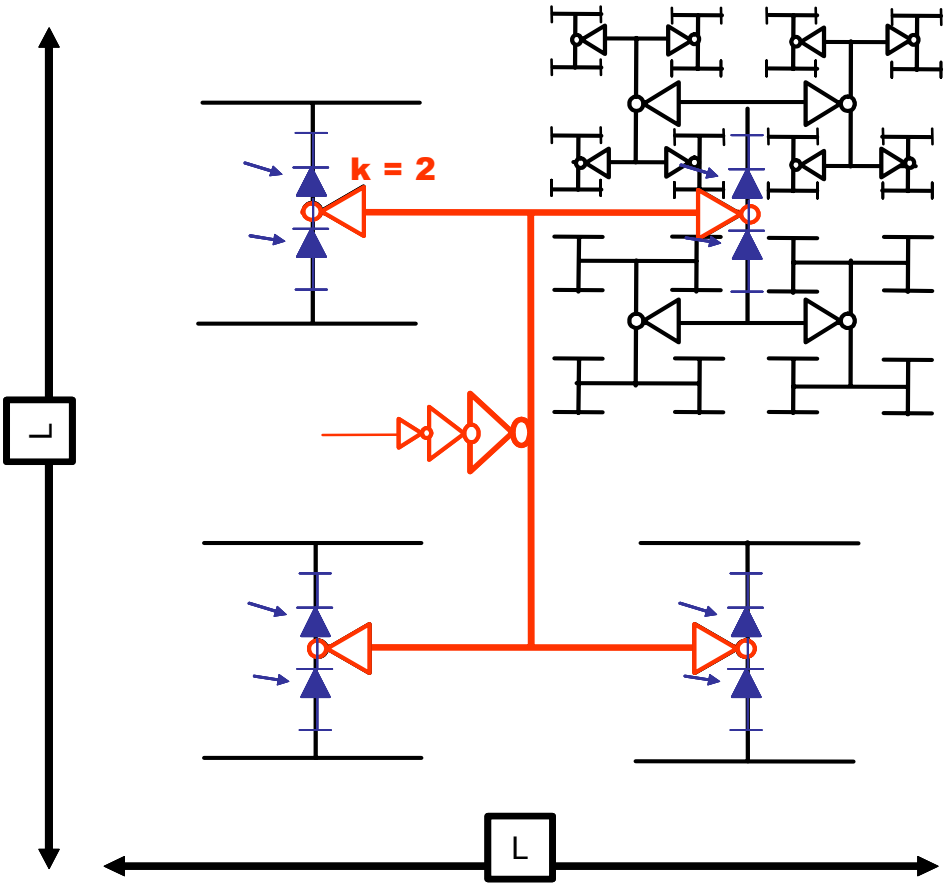


Figure 3.3 Optical clock injection to level $k = 2$

Similarly, the delay along a path from the laser to a leaf repeater[2] can be calculated by subtracting the delay of the top *k* repeaters and *k-1* wires from equation (3.9) and adding the delay $t_{Det}$ of the photo-detector:

$$t_{delay,Optical,k} = (n-k)t_{FO4} + t_{Det} + \frac{C_W R_W L^2}{6}\left(\frac{1}{4^{k-1}} - \frac{1}{4^{n-1}}\right) \quad \textbf{(3.13)}$$

Ultimately, the limiting factor in optical clock injection is the laser power available. The amount of laser power required to do optical clock distribution to level *k* depends on the optical-to-electrical conversion efficiency and the capacitive load to be driven by the laser:

$$\begin{aligned} P_{laser} &= 2\frac{hc}{\eta q \lambda} V_{dd} \cdot f \cdot C_{laserload} = 2\frac{V_{dd} \cdot f}{R} C_{laserload} \\ C_{laserload,k} &= 4^{k-1} C_{Det} + 4^k C_{in,k+1} + 3/2 \cdot 2^{k-1} L C_W \\ &= 4^{k-1} C_{Det} + 4^k C_{in} + \frac{3}{2} C_W L \cdot 2^k \left(1 - \frac{1}{2^{n-k}}\right) \end{aligned} \quad \textbf{(3.14)}$$

Here, *h,c,η,q* and $\lambda$ are Planck's constant, the speed of light, detector quantum efficiency, electronic charge and optical wavelength respectively. *R* is the detector responsivity which is ~ 0.5 A/W (assuming $\eta = 0.8$, and $\lambda = 850$ nm) in this chapter. Equations (3.12) - (3.14) can now be graphed in the context of realistic CMOS chips.

### 3.2.1. 1-GHz Microprocessor in a 0.18 µm CMOS Process

Intel's McKinley microprocessor, which is a version of the Itanium™, Intel's high end server processor, will be the starting point for the comparison of optical and electrical

[2] Note that the propagation delay of the light beams in air is not relevant because it is not subject to creating jitter like the other delays. There is no mechanism for added noise in a longer optical path vs. a shorter one.

clocking in a 1 GHz microprocessor application [2]. The McKinley was fabricated in a 0.18 μm process with six aluminum wiring layers. The core clock ran at 1 GHz and clocked a total of 157,000 latches. The distribution was realized by a balanced multi-level H-tree. The supply voltage ranged from 1.2 – 2.0 Volts with corresponding clock frequencies of 1.2 GHz – 2.0 GHz. At 1 GHz, the full chip consumed 130 W of power, with the H-tree clock distribution consuming 30 % of that total.

The parameters used in this model are summarized in Table 1.The main assumption is that the total clock load is 8 nF, comprising the input capacitance of ~ 160,000 latches and connecting wires. That equates to ~ 50 fF input capacitance per latch including final wires, which is probably a reasonable or slightly high estimate. It is also assumed that each repeater at the last level drives 10 latches so that there are 16,000 end points for the clock tree. Given the geometrical fan-out of 4, that leads to an $n = 8$ level tree. The leaf repeater capacitance is then easily calculated from equation (3.10). The remaining electrical parameters are based on published values [5]. The FO-4 delay characteristic of Intel's 0.18 μm technology is used. The resistance per unit length of all the wires is assumed equal to that of low resistance global wires and the wire capacitance per unit length, which does not vary significantly between local, semi-global or global wires, is assumed to be an ideal 0.2 pF/mm.

Table 3.1 Model parameters for 1 GHz microprocessor in 0.18 μm CMOS

| | Symbol | Value |
|---|---|---|
| Clock frequency | $f$ | **1 GHz** |
| Supply Voltage | $Vdd$ | **1 V** |
| Final wire and latch | $C_{load}$ | **8 nF** |
| Leaf node repeater | $C_{in}$ | **122 fF** |
| Wire capacitance/unit length | $C_W$ | **200 fF/mm** |
| Wire resistance per unit length | $R_W$ | **20 Ω/mm** |
| Fan-out of 4 delay | $t_{FO4}$ | **50 ps** |
| Chip total dimension | $L$ | **20 mm** |
| Detector rise/fall time | $t_{Det}$ | **10 ps** |
| Receiver-less detector | $C_{Det}$ | **30 fF** |

Fig. 3.4 plots the clock delay for the optical clock distribution case (equation (3.13)) versus level of optical insertion. On the plot a horizontal line at 0.78 ns shows the total clock tree delay (equation (3.9)) of the conventional electrical distribution model. As marked on the figure, 1W of optical power from a laser allows receiver-less injection up to the 5$^{th}$ level in the H-tree, which corresponds to 256 injection points and results in a 78 % delay savings. As discussed in Chapter 2, clock delay is proportional to the jitter and skew in the distribution, hence the reduction in delay will result in a corresponding reduction in worst case jitter and skew.

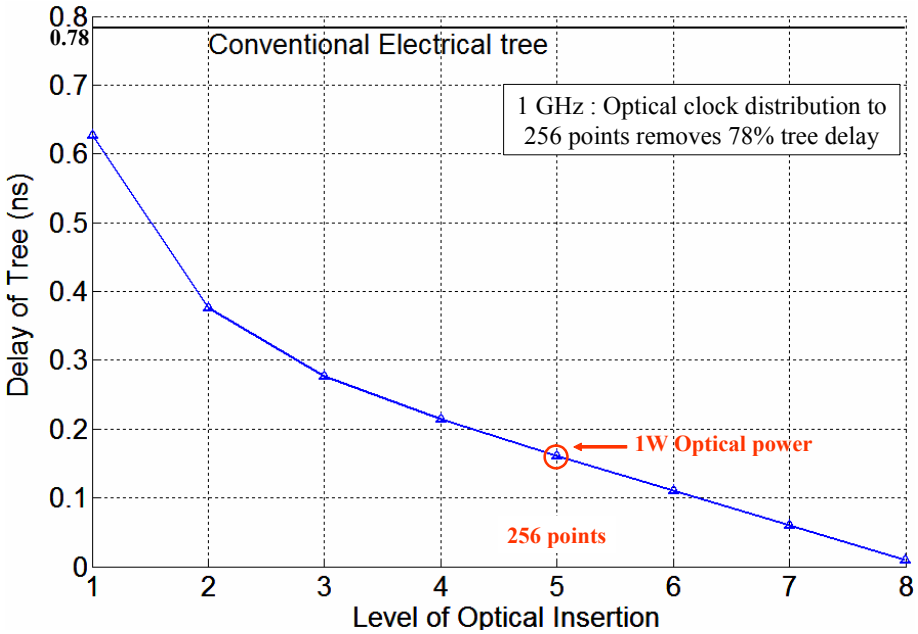


Figure 3.4 Total clock delay vs. level of optical clock injection for 1 GHz H-tree

Note that the conventional electrical tree delay of 0.78 ns corroborates reasonably well with published total tree delays for 1 GHz microprocessors [6]. Other heuristics of the model which corroborate with microprocessor distributions are that wire delay is ~ 34 % of total delay and that power consumption in the distribution is ~ 30 % of total power consumption.

Another potential advantage of optical clocking is that it may eliminate some of the power consumed in the distribution, which was just noted to be ~30 % of the total chip power. Optical clock distribution, as modeled here, can only remove a fraction of that, depending on the level of insertion and the photo-detector capacitance. Fig. 3.5 plots equation (3.12) for different photo-detector capacitances. To reduce the distribution power consumption to 10 % of the all-electrical case, optical injection to the last level, with very low capacitance detectors, is required. Fig. 3.6 plots equation (3.14), the laser output power required to inject to a certain level. A practical upper bound on laser output

power is ~ 1 W. Thus, as circled, optical insertion beyond level 5 would be impractical with receiver-less detectors.

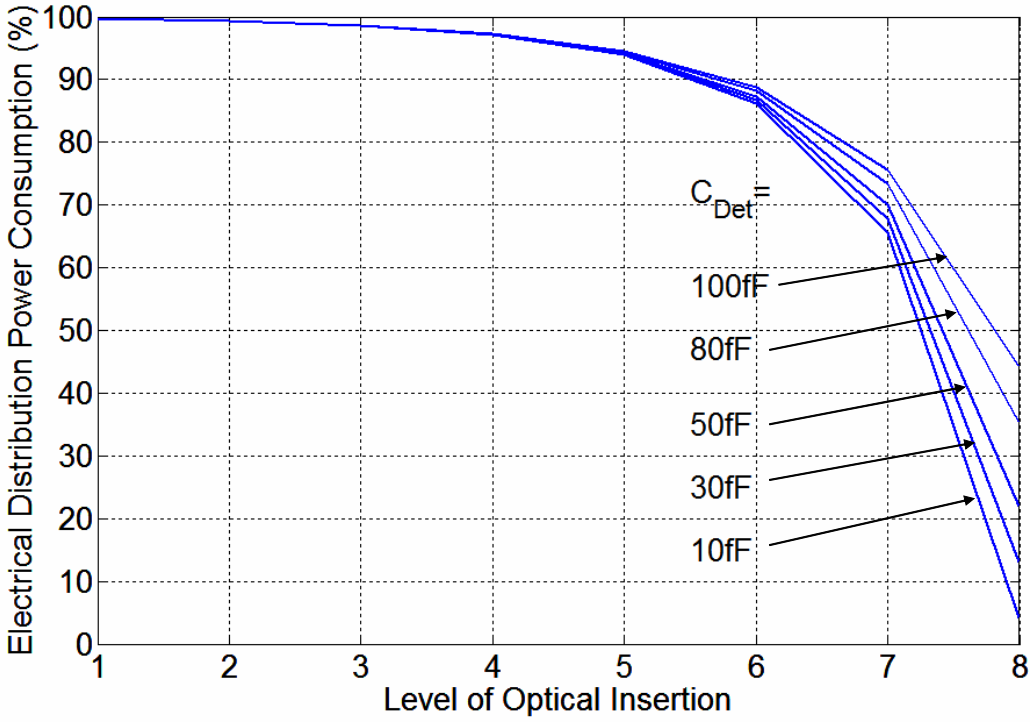


Figure 3.5 Electrical power consumption vs. level of optical injection for different photo-detector capacitances (1 GHz)

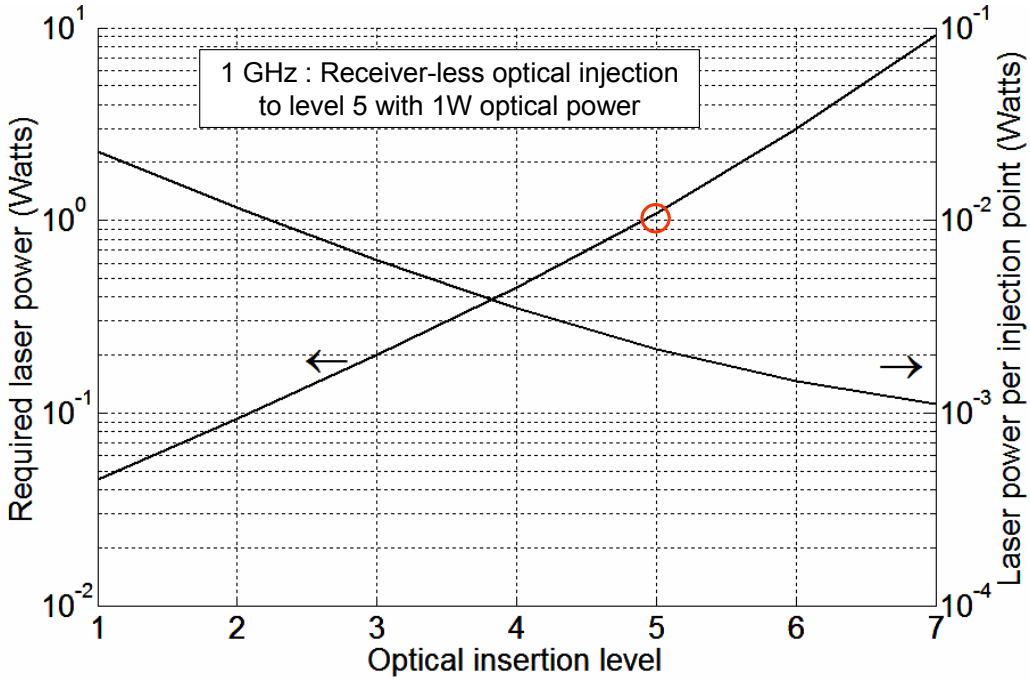


Figure 3.6 Laser output power required for optical clock injection vs. insertion level. (Right) Laser power required per injection point (1 GHz)

Based on the above graphs, the primary advantage of optical clock injection is reduction in delay and the resulting saving in jitter and skew. The analyses presented were for receiver-less clock injection; however, a simple extension to this model views receivers as capacitive gain stages which allow deeper injection into the tree for the same laser power budget[3]. For example, a good receiver may provide a capacitive gain of 10 X, implying that both curves in Fig. 3.6 would shift down by 10 X, allowing optical injection to the 7$^{th}$ level with 1W of laser power. However, a receiver would add ~ 2 FO-4 delays (100 ps) to each path. With reference to Fig.3.4, there would be no net latency benefit from injecting to levels 6 or 7 with receivers. Obviously, receivers would also increase power consumption.

[3] This assumes the detector capacitance is not the dominant capacitance at any level, which is a valid assumption, given the values of $C_{in}$ and $C_{Det}$ in Table 1.

### 3.2.2. 10-GHz Microprocessor in a 0.022 μm CMOS Process

This section extends the above analysis to a 10 GHz microprocessor using CMOS technology predictions for the year 2008 from the International Technology Roadmap for Semiconductors (ITRS) [7]. In 2008, 22 nm CMOS should enable $t_{FO4} = 11$ ps (500 * $L_{drawn}$, [5]), and $f$ = 10 GHz. Supply voltage and total chip power are expected to remain fixed at 1 V and ~ 200 W. Wire capacitance remains roughly fixed. Wire resistance may increase, but is optimistically assumed fixed to the low global wire resistance as in the 1 GHz, 0.18 μm case. The parameters used in the 10 GHz, 0.022 μm model are summarized in Table 2.

Table 3.2 Model parameters for 10 GHz microprocessor in 0.022 μm CMOS

| | Symbol | Value |
|---|---|---|
| Clock frequency | $f$ | **10 GHz** |
| Supply Voltage | $Vdd$ | **1 V** |
| Final wire and latch | $C_{load}$ | **16 nF** |
| Leaf node repeater | $C_{in}$ | **15.38 fF** |
| Wire capacitance/unit length | $C_W$ | **200 fF/mm** |
| Wire resistance per unit length | $R_W$ | **20 Ω/mm** |
| Fan-out of 4 delay | $t_{FO4}$ | **11 ps** |
| Chip total dimension | $L$ | **10 mm** |
| Detector rise/fall time | $t_{Det}$ | **10 ps** |
| Receiver-less detector | $C_{Det}$ | **30 fF** |

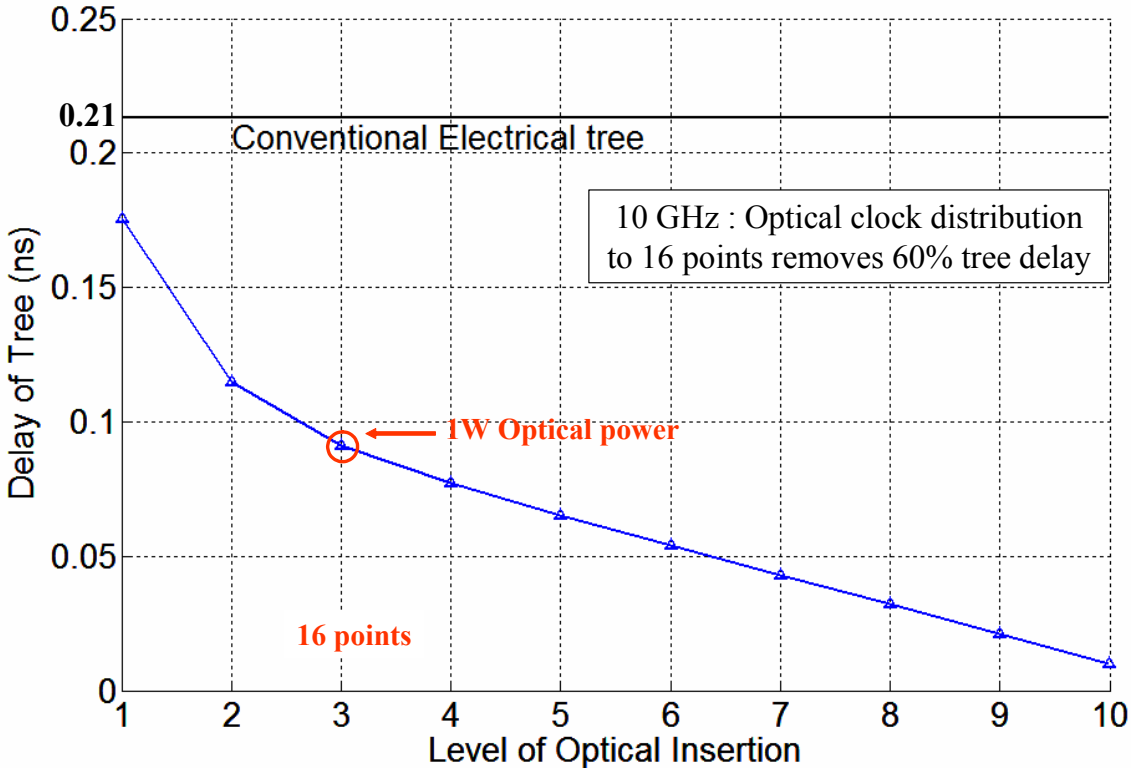


Figure 3.7 Total clock delay vs. level of optical clock injection for 10 GHz H-tree

The main assumption is that the number of latches on a 10 GHz microprocessor increases to 2.6 million. The capacitance per latch including connecting wires for the 0.18 µm technology in Section 3.2.1 was ~ 50 fF. Relative to the 0.18 µm technology, 0.022 µm CMOS represents a shrink factor $\alpha = 1/8$. Using a simple parallel plate model for a latch, if all dimensions shrink by $\alpha$, the latch capacitance shrinks by $\alpha$ i.e. it becomes $50/8 \approx 6.25$ fF. With 2.6 million latches the total clock load[4] comes to ~ 16 nF. In 0.18 µm CMOS the load was 8 nF and the chip area was 400 mm$^2$. In 0.022 µm CMOS the gate capacitance per unit area is 8 times greater, so a 16 nF load will occupy a 100 mm$^2$

[4] It is difficult to predict what the load would be at 10 GHz and 16 nF might be too large because a 10 X increase in clock frequency and 2 X increase in clock load could raise the switching power by 20 X, whereas according to ITRS, chip power remains fixed. However, future chips are expected to lower switching power by selectively "gating" parts of the clock tree and by using other low power techniques.

area, i.e. the chip will be 10 mm by 10 mm. As before, each repeater at the last level drives 10 latches so that there are 260,000 end points for the clock tree. Given the geometrical fan-out of 4, that leads to an $n$ = 10 level tree. The leaf repeater capacitance is then easily calculated from equation (3.10).

Fig. 3.7 plots the clock delay versus level of optical insertion at 10 GHz. The conventional electrical delay is 0.21 ns or ~ 2 clock cycles, which is reasonable. The other heuristics of the model remain the same as in the 1 GHz case. However, from Fig. 3.9, 1W of laser power allows receiver-less injection only up to the 3rd level, which corresponds to 16 injection points and results in a 60 % delay savings. Fig. 3.8 shows that 20 fF or lower photo-detector capacitance is required to keep the added power consumption from detectors minimal.

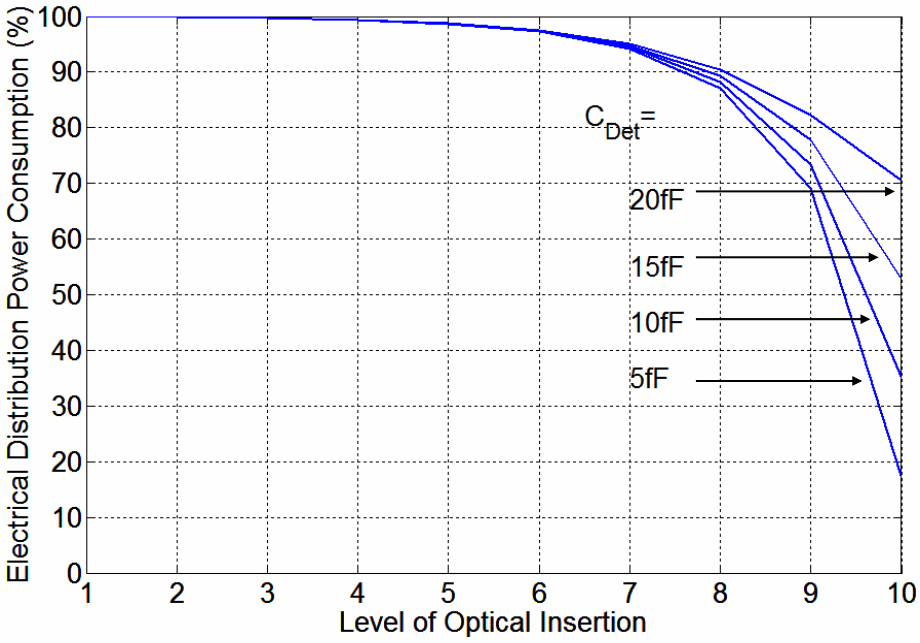


Figure 3.8 Electrical power consumption vs. level of optical injection for different photo-detector capacitances (10 GHz)

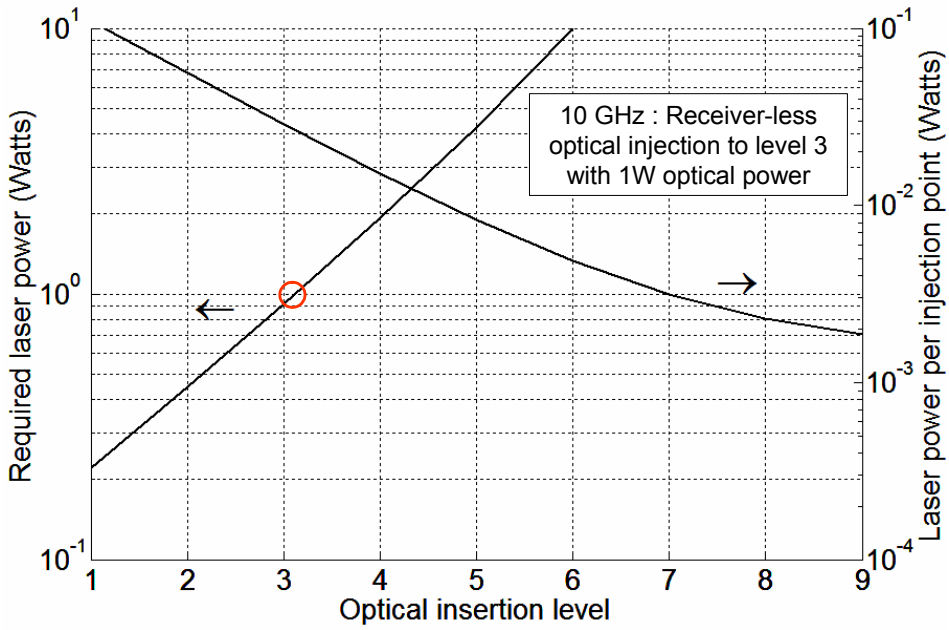


Figure 3.9 Laser output power required for optical clock injection vs. insertion level. (Right axis) Laser power required per injection point (10 GHz)

The latency benefit of optical clock distribution at 10 GHz is less and requires lower detector capacitance than in the 1 GHz case. However, maintaining wire resistance and capacitance at their 0.18 μm technology values may also involve some tradeoffs. In particular, more repeaters than are included in this model may be needed. Additionally, since jitter and skew margins at 10 GHz are proportionally lower, latency reduction may be quite important. Overall, the quantitative model of clock distribution developed here suggests the following:

- Optical clock distribution can remove a significant fraction of the clock latency on a large chip resulting in lower jitter and skew. Optical clock distribution, as presented, does not significantly lower the electrical power consumption of a large chip.
- The number of injection points required for significant latency savings are in the range of 10's to 100's, and are practical.

- Detector capacitance of order 10 fF is required for power efficient optical clocking.
- The total laser output power determines the amount of latency savings possible, and in general as clock frequency increases less optical energy is available. Therefore:

  A smaller clock load can be clocked very precisely OR

  A large clock load can be clocked with less precision
- Receiver amplifiers allow deeper insertion of optics into a conventional H-tree. However, the latency benefit of deeper insertion is almost entirely offset by the added receiver latency.

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# Chapter 4

# Receiver-less Optical Clocking with Flip-Chip Integrated Photo-detectors

The first objective of this dissertation was to quantify the theoretical benefits of optical clocking. That has been addressed in Chapter 3. The remainder of this dissertation shows the feasibility of optical clock injection through a series of three experiments. In the first experiment, described here, a low jitter optical clock is injected into a digital CMOS circuit using hybrid integrated receiver-less photo-detectors.

## 4.1. Background on Photo-detectors for Clocking

The limiting parameter in a receiver-less distribution is the total power available from the mode-locked laser. To minimize power it is important to have a low loss distribution and low capacitance photo-detectors. The capacitance of detectors is inversely proportional to the width of the high field region. For P-I-N detectors this width is the width of the intrinsic or depletion region and for metal-semiconductor-metal (MSMs) detectors it is the finger spacing. Increasing this critical dimension however, lowers the field and can make the detector slower, unless greater bias voltages are available. Capacitance can also be reduced by any field reducing mechanism such as the use of insulating substrates. For a given design, capacitance scales with detector size, and size is limited by the practical ability to focus light to spots smaller than 5 to 10 μm diameter.

Photo-detectors can be hybrid-integrated to CMOS chips after chip fabrication via a number of techniques [1, 2]. The detector integration scheme affects the parasitic capacitance, footprint and density of the front-end. The advantage of hybrid integration is that the material and design of the photo-detector is independent of the transistor technology. On the other hand, monolithic CMOS photo-detectors fabricated along with circuits in silicon have the promise of greater density, superior cost and lower parasitics. But, the doping and material parameters in CMOS processes typically imply detectors with either poor speed or poor responsivity at 850 nm [3].

The most mature hybridization techniques are wire bonding and flip-chip bonding. The performance tradeoffs between these two techniques have been described [1]. Wire bonding has greater parasitic inductance and capacitance, reducing performance at high bit-rates as compared to flip-chip bonding. Wire-bonded off-the-shelf P-I-N detectors

present a front-end capacitance in the range of 200 fF or higher depending on detector size. Flip-chip bonding is potentially a wafer-scale manufacture-able technology enabling the integration of large device arrays. Hence flip-chip bonding is more suitable for high-performance applications requiring minimum front-end capacitance. The measured capacitance of 15 μm x 15 μm flip-chip bonded GaAs P-I-N detectors was reported to be ~ 52 fF [4]. The capacitance of flip-chip bonded photo-detectors can be reduced to ~ 10 fF by reducing their pad area to nearly 5 μm x 5 μm, which is ultimately limited by the need for tight focusing and better alignment. Note that MSM detector designs have similar capacitance (depending on finger spacing) but dark currents tend to be of order nA vs. pA for P-I-N detectors.

## 4.2. Receiver-less Operation and Advantages

Receiver-less optical clocking refers to the technique of creating rail-to-rail voltage swings at a high impedance electrical node by shining light from a pulsed laser onto a pair of optically differential photo-detectors that directly charge and discharge the clocked node. Receiver-less operation has not been the norm in prior optical clocking research, where photo-detectors are typically followed by gain stages which amplify the photo-generated current or resultant voltage to full swing. The approach presented here is called receiver-less because it does not use amplifiers or receivers, and relies instead on delivering sufficient optical energy to the photo-detectors to fully charge and discharge each node.

As shown in Fig. 4.1 each receiver-less injection node consists of two photo-detectors in a series or totem-pole configuration, that drive a high impedance circuit such as the gate of a CMOS transistor. The pulse train from a mode-locked laser is split into two

beam paths, one of which is delayed by half the repetition period or T/2. The two beams are separately focused onto the two detectors. The shifted pulses alternately charge and discharge the high impedance node through the detector photocurrent, generating a square wave clock of adjustable duty cycle. If the optical power per detector is sufficient to charge the detector and load capacitances then the injected clock voltage is full swing. The detectors limit the swing of the node in the middle to one built-in voltage above and below the supplies[1].

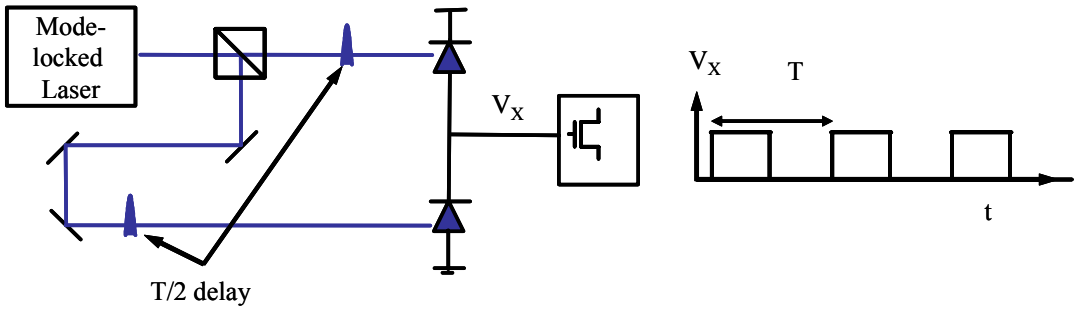



Figure 4.1 Receiver-less square wave clock generation at a high-impedance node ($V_x$) using optically differential delayed mode-locked laser pulses

The advantage of the receiver-less approach is that it minimizes the latency from the clock source to the optically clocked node, limiting it to the detectors' response time. Placing receivers after the photo-detectors would add circuit delay to the path and introduce some electrical power consumption per receiver. The analysis in Chapter 3 showed that latency reduction and associated jitter and skew reduction are likely the primary benefits of optical clocking. The receiver-less approach has the potential to maximize this benefit, while minimizing the electrical power consumption since the only electrical power consumed is that required to charge the load plus detector capacitance.

[1] This is because the voltage over a diode cannot rise above the built-in voltage in forward bias.

The lack of multiple gain stages implies there are fewer supply noise injection points and less degradation from circuit related mismatch or offset. Finally, another noise advantage of this approach is that the signal swing is large so the impact of noise from supply, substrate or other sources is small compared to the signal.

A separate feature of receiver-less clocking is that if the photo-detectors are fast enough, very sharp transition times can be created directly on-chip. Because there is no receiver, the transition times can be faster than the rise time of a CMOS inverter. Sharp rise times can be used for sampling and triggering circuits where timing accuracy is required. Detector rise times ~ 10 picoseconds are practical.

The limitation in receiver-less clocking is the amount of optical power required from the laser to clock a significant capacitive load. At present, lasers can economically emit no greater than ~ 1 W of total optical power at any repetition rate ranging from MHz to tens of GHz [5]. Poor power conversion efficiency makes higher power lasers impractical. The capacitive load that can be driven by 1 W of optical power is:

$$C = \frac{I}{f \cdot V} = \frac{R \cdot P_{opt}}{f \cdot V} \tag{4.1}$$

where $R$ is the photo-detector responsivity in Amperes/Watt of optical power, $P_{opt}$ is the optical power in Watts, $f$ is the clock frequency, $V$ is the clock voltage swing and $C$ is the load that can be driven. Practical responsivities for hybrid photo-detectors are ~ 0.5 A/W. Assuming a voltage swing ~ 1 V, an optical power of 1 W can drive a load equal to $\frac{0.5}{f}$ nF where $f$ is in GHz, that is, 0.5 nF of load can be driven at 1 GHz, or 0.25 nF at 2 GHz. Thus, potential applications for optical clocking are likely limited to those requiring high precision clocks delivered directly to relatively small capacitive loads. Additionally

low capacitance, high responsivity, highly integrated photo-detectors will be required. It can be noted that the area penalty of receiver-less optical clock injection is small. Detector area is typically limited by the ability to focus or otherwise channel light into a small region. Detector and laser spot sizes with 5 μm diameter are practical. Thus, even with ten thousand detectors on a 2 cm x 2 cm chip, the area penalty is ~ 0.05 % of the total chip area.

In summary, receiver-less optical clock distribution may be able to reduce the jitter, skew and electrical power of traditional repeatered-wire approaches, but the number of receiver-less distribution points is limited by the optical power budget and detector capacitance. A reasonable assumption for present flip-chip technology might be 20 fF, and if that were the dominant load, it would allow ~ 1000 differential receiver-less points at 10 GHz with 1 W optical power. The following sections describe experiments in high precision optical clock injection to small load capacitances using flip-chip integrated GaAs P-I-N photo-detectors.

## 4.3. CMOS Design and Flip-Chip Integration of Photo-Detectors

The operation of a CMOS digital logic block clocked by receiver-less injection of optical pulses from an 80 MHz Ti:sapphire mode-locked laser was shown. The CMOS logic was fabricated in a 0.5 μm ultra-thin silicon-on-sapphire (UTSi) process from Peregrine semiconductor [6]. The circuits in this process benefited from reduced parasitic capacitances due to the insulating substrate. Hence transistor speeds in this process were nearly equivalent to those in a 0.25 μm bulk process. The commercial bench-top Ti:sapphire laser from Spectra-Physics Inc generated pulses of about 100 fs width, much

smaller than any time-scale on the chip. The laser light was split into two beams by a beam splitter and used to drive a totem-pole of detectors for direct clock injection. Pulses from the two beams were temporally offset by 6.2 ns to generate a 50 % duty-cycle clock on chip.

As shown in Fig. 4.2 the circuit to be clocked consisted of four static D-flip-flops and an XOR gate connected to form a small pseudo-random-bit-sequence (PRBS) generator. This closed loop circuit does not require an input, and runs by itself while it receives a good clock. The output of one of the flip-flops was routed to a wire bond pad and observed on a 20 GHz digital channel analyzer (DCA) - oscilloscope from Agilent Technologies. A single-ended buffer-chain and source follower were used to provide sufficient current to drive the DCA. The chip interfaced with the external world via a wire bonded package and printed circuit board with impedance matched lines, and was connected to the DCA with SMA cables. Approximate values for the bond-wire capacitance and inductance are indicated on the figure.

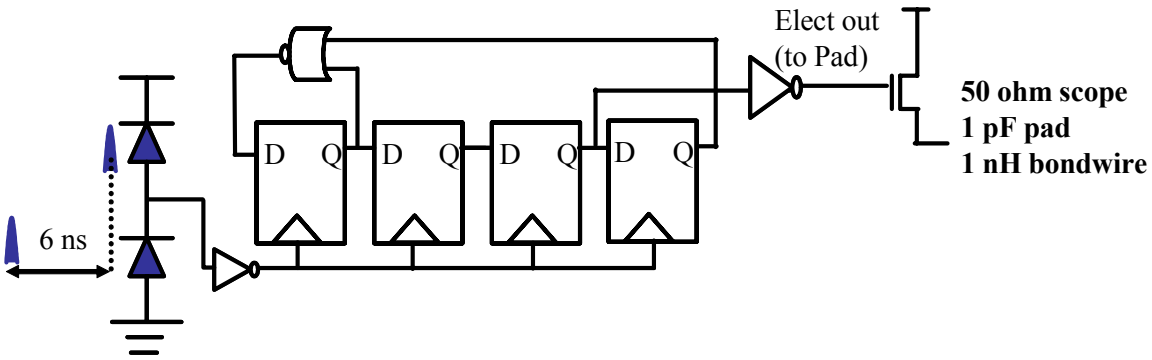
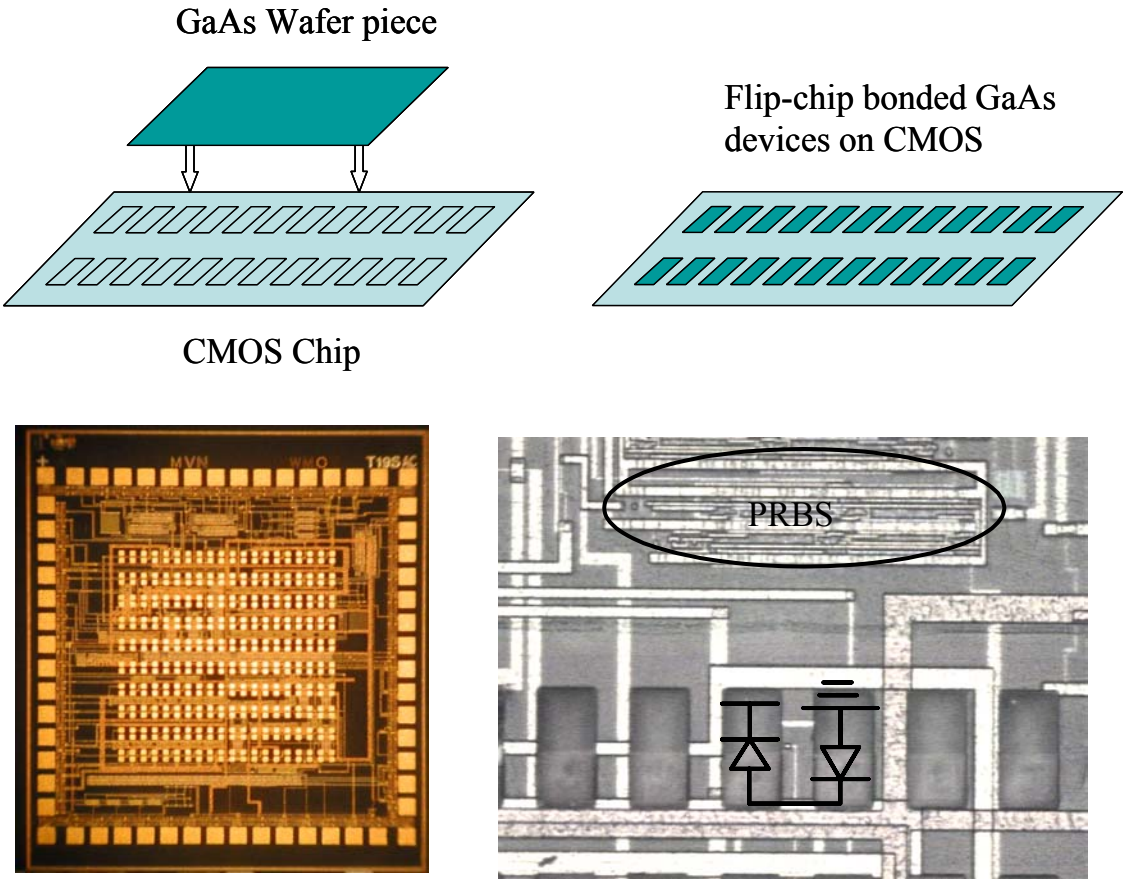



Figure 4.2 Pseudo-random-bit-sequence (PRBS) circuit with receiver-less optical clock. PRBS output viewed on scope after source follower, wire-bond and SMA cable

The photo-detectors in the totem-pole were dual purpose modulator/photo-detector devices fabricated separately on a Gallium Arsenide (GaAs) wafer and then integrated

onto the CMOS chip via flip-chip bonding. The modulator/photo-detector had a basic P-I-N structure with ~ 1-2 μm thick intrinsic region nominally containing 50 pairs of 95 Å wide GaAs multiple-quantum-wells (MQW) and 30 Å wide $Al_{0.3}Ga_{0.7}As$ barriers. When a modulated reverse bias is applied to this device its absorption characteristic changes with bias, for wavelengths near 850 nm. This quantum-confined-stark-effect (QCSE) leads to the modulation function which has been studied and reported elsewhere [7]. In this experiment, a constant 3.3 V reverse bias was applied to the device so that it behaved only as a reverse biased P-I-N photo-detector.

The flip-chip bonding technique used to integrate the GaAs based modulator/photo-detectors with the CMOS chip was initially developed elsewhere [8]. A brief overview of the process steps used to integrate the devices in this work is given here. Appropriately doped GaAs/AlGaAs layers were grown on a GaAs wafer via molecular beam epitaxy (MBE) and the wafer was then processed to define an array of 200 isolated device mesas [9]. Indium was evaporated and patterned onto the P and N contacts of each of the devices to provide the bonding material. A corresponding array of bonding pads had been designed and fabricated on the CMOS chip during the foundry run. After fabrication gold was evaporated on these bonding pads to enable indium-gold bonding. As shown conceptually in Fig. 4.3 (a) and (b) the GaAs chip and the CMOS chip were laid vertically atop each other and bonded using a combination of pressure and temperature in a commercial flip-chip bonder. Epoxy was inserted into the bond via capillary action to ensure mechanical stability. Thereafter, the GaAs substrate was removed chemically, leaving an array of 200 individual photo-detectors for interfacing with the CMOS chip optically.

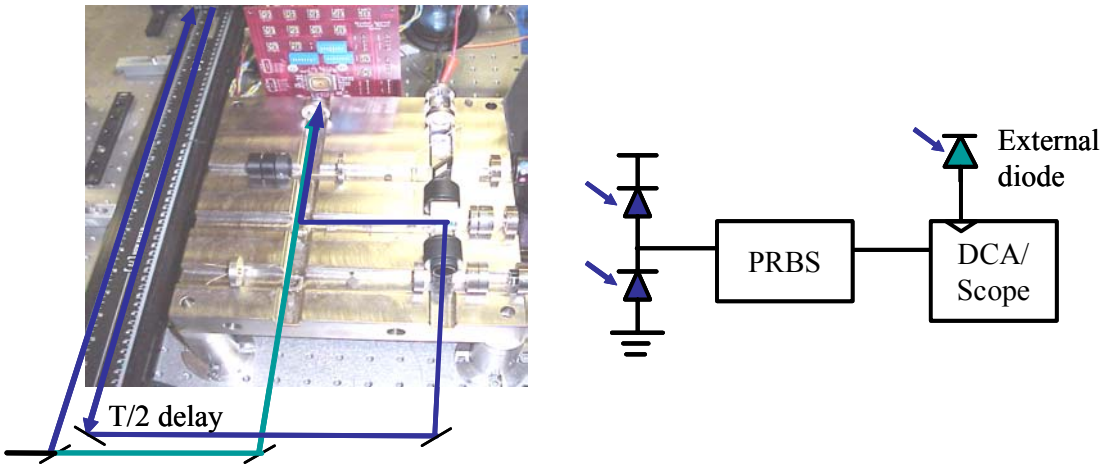



(a) before bonding (b) after bonding

Figure 4.3 Conceptual diagram of the flip-chip bonding process (top row). Microscope photographs of the CMOS chip before and after bonding (bottom row). The PRBS and photo-detectors are marked on the zoomed-in photograph of the chip after bonding

The flip-chip bonded photo-detectors were fabricated as rectangles approximately 40 µm x 80 µm in size to allow reuse of existing lithography masks, but the active area of the detectors was reduced to a square 12 X 12 $\mu m^2$. The capacitance of the photo-detectors was ~ 30 - 50 fF per detector for this active area. In the future this capacitance could probably be reduced to ~ 10 fF by shrinking the active area to 6 X 6 $\mu m^2$. The responsivity of the photo-detectors was 0.2 A/W, measured using the Ti:sapphire short

pulse laser. The optical clock drove a small buffer which provided capacitive gain to drive the four flip-flop inputs. The total load on the receiver-less node was ~ 100 fF




(a) Photograph of optical set up (b) Schematic of measurement set up

Figure 4.4 Photograph and schematic diagram of the experimental set-up

## 4.4. Experimental Results and Discussion

The free-space optical set-up and the chip, mounted on a printed-circuit-board, are shown in Fig. 4.4 (a). The two clock beams are drawn in. Fig. 4.4 (b) shows a schematic where the two optical beams are shown impinging on the receiver-less totem-pole which drives the PRBS, whose output is measured on the DCA/scope. The scope itself is triggered by the same laser via an external commercial photo-detector.

Fig. 4.5 shows the experimental result that demonstrates a stable, functioning optically clocked digital circuit, and measures an upper bound on the jitter of its output data. The plot shows zoomed-in and zoomed-out versions of the eye-diagram on the oscilloscope when 160 μW of optical power is shone on each detector. Equation (4.1) yields the required optical power to drive a 100 fF load full swing to 3.3 V, at 80 MHz using photo-detectors with 0.2 A/W responsivity to be 130 μW, which is close to the measured value.

The extra power maybe due to detector responsivity variation or, perhaps more likely, because the voltage swing was larger than 3.3 V. Note that the receiver-less node can swing up to one built-in voltage (~ 1.4 V for GaAs) beyond the rails in both directions.

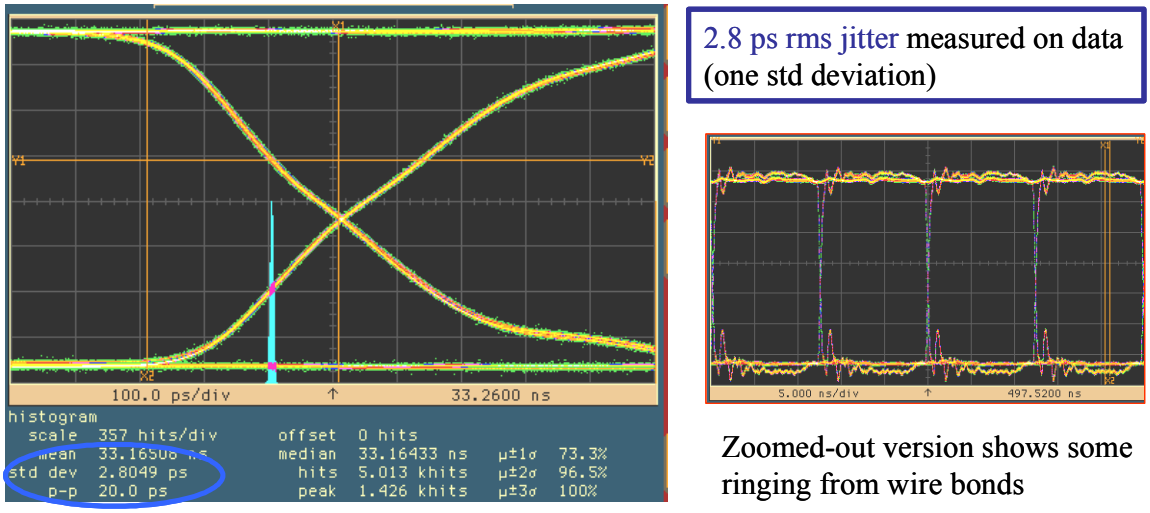



Figure 4.5 Zoomed-in picture of eye diagram of the output of the PRBS driven by the optical clock. The histogram of the jitter on the falling edge is shown. A zoomed out version is also shown

The zoomed-in picture in Fig 4.5 shows a histogram on the falling edge of the flip-flop output. The histogram measures the statistics of the time when this edge crosses a given voltage. The rms jitter or one standard deviation of the histogram was less than 3 ps when observed over 5000 hits. Clock jitter would directly increase the measured rms jitter, thus, this measurement indicates that the jitter on the injected clock is below 3 ps.

The measured jitter is a combination of jitter on the clock as well as any jitter from the circuit, board and measurement set-up. The clock jitter is comprised of a) the jitter of the laser itself, and b) jitter from the buffer immediately following the photo-detectors, which could be affected by the rise time of the photo-detectors. The laser jitter was measured optically in a separate optical cross-correlation experiment described in Chapter 6. The measured laser jitter was less than 300 fs rms. However, the photo-detector rise and fall

times were found to be nearly two hundred picoseconds long, due to carrier trapping in the multiple-quantum-wells. The switching times were measured (see Appendix 4.1) using an optical pump-probe technique similar to that described in Chapter 5, and were found to be between 100 - 200 ps at 3.3 V bias. These times corroborate approximately with previously published 10 % - 90 % switching times of ~ 200 ps for a similar quantum well structure with 35 Å barriers, at an applied bias of 5 V [10]. As reported in [10], the carrier sweep out times could be reduced to ~ 90 ps by raising a voltage across the device to 10 V, however this was not attempted here. Long carrier trapping times were a side-effect of using quantum-well based P-I-N devices to leverage the modulator functionality. A simple P-I-N detector would likely have been better.

The circuit jitter is comprised of noise from the flip-flops, and the source follower. The rest of the chip could couple power supply noise to the PRBS output, however, no other circuitry on the chip was active during the measurement. Though the decoupling capacitance on-chip was minimal, there was decoupling on the board, and jitter on the external power supplies was likely insignificant. The oscilloscope jitter was measured to be ~ 800 fs rms. Therefore, the excess jitter measured is expected to be a result of the long photo-detector rise time, and the corresponding uncertainty in switching times for the subsequent clocked nodes. Future use of ordinary P-I-N photo-detectors could reduce the measured jitter in this experiment to the intrinsic jitter of the scope. A lower jitter measurement was achieved in this research by using ordinary P-I-N detectors as reported in Chapter 6.

In summary, direct injection of short pulses from a mode-locked laser to a CMOS digital circuit without the use of optical clock receivers has been shown. The experiments

demonstrate the feasibility of optical clock injection using hybrid integrated photo-detectors. The clock injection resulted in a 2.8 ps rms jitter measurement on the output of the clocked circuit. The photo-detectors were low capacitance, being in the range of 30 - 50 fF, and had a short pulse measured responsivity of 0.2 A/W. The optical power required for the experiment was commensurate with calculations. The speed of the photo-detectors and hence, perhaps, the measured jitter number was limited by carrier escape times in the quantum wells, an effect that might be avoided through the use of ordinary P-I-N diodes.

# References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# APPENDIX 4.1 Optical Pump-Probe Measurements of MQW Detector Transition Times

An optical pump-probe measurement was used to view the voltage at the clock injection node and thereby measure the transition time of the MQW photo-detectors. Figure 4.6 is a schematic of the set-up. In this experiment the MQW devices functioned as conventional photo-detectors. In addition the modulator functionality of the top diode was used to optically sample its voltage. The laser beam was divided into three paths, two of which clocked the PRBS. The third was a low power probe that optically sampled the voltage on the top MQW diode. As explained further in Chapter 5, this pump-probe experiment used the quantum confined stark effect in the MQW diode to convert the electrical voltage on the diode to an optical signal observed in the light reflected from the diode. By varying the delay between this probe and the pump on the bottom diode the clock edge was sampled with sub-picosecond accuracy. This is shown in Figure 4.6 for two pump powers. The 90 - 10 % fall time of the clock is between 100 - 200 ps for the applied bias of 3.3 V. In a simple P-I-N with 1 μm I region, the rise time would be expected to be ~ 30 ps with a bias of ~ 3 V. The fall times measured here may be limited by carrier sweep out times in the quantum wells.

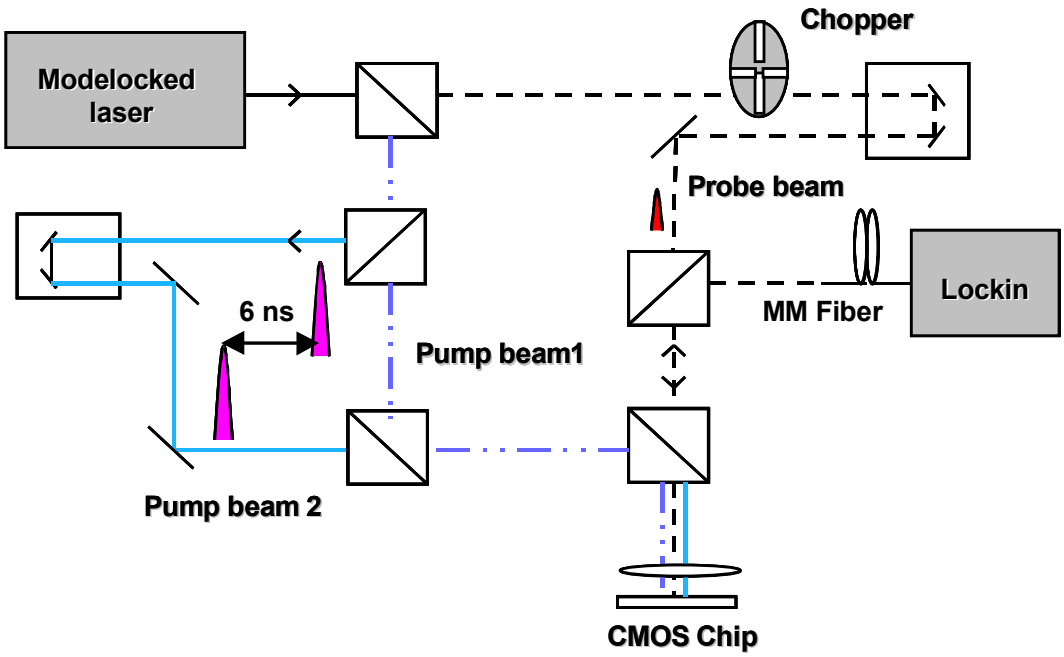



Figure 4.6 Schematic of three beam optical pump-probe set up to measure MQW detector transition time

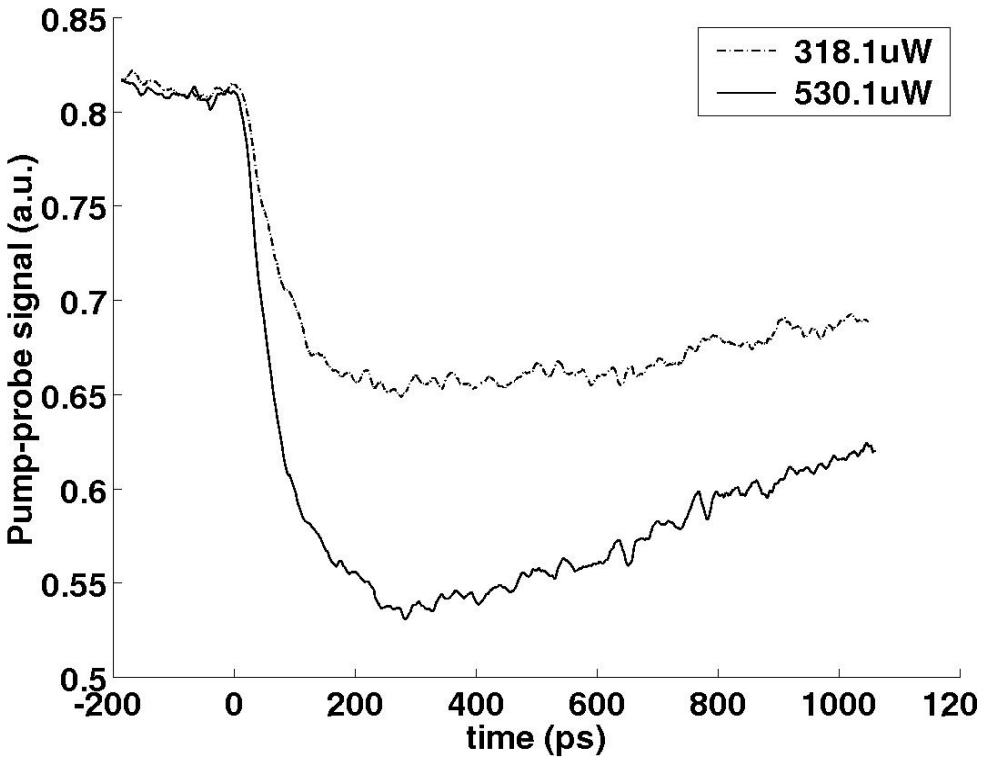



Figure 4.7 Pump-probe measurements of falling edge at the clock input to PRBS clocked by MQW detectors. Powers are per detector; 318 µW and 530 µW are shown

# Chapter 5

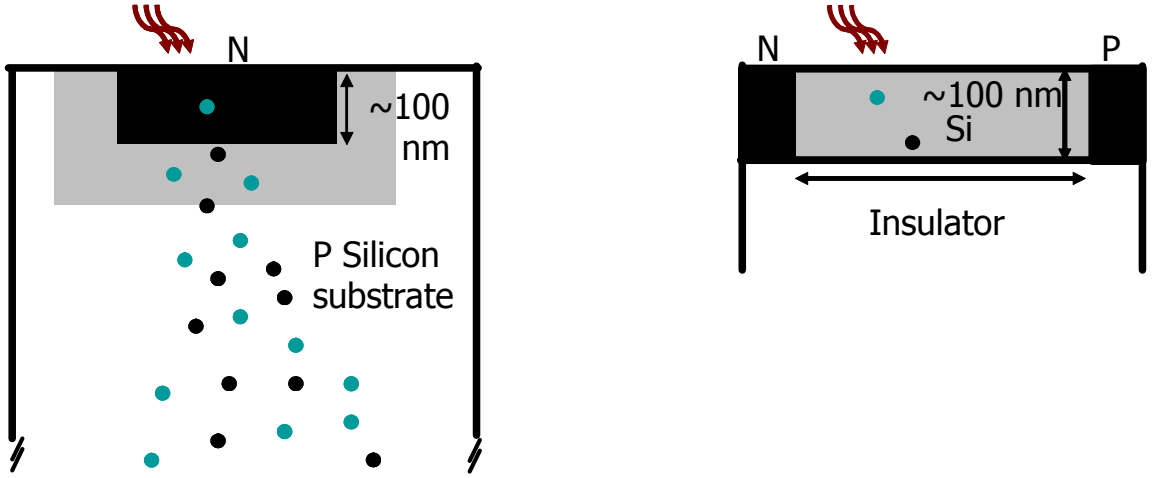
# Receiver-less Clocking with Monolithic CMOS Detectors and Blue Light

The ability to fabricate useable photo-detectors in production line CMOS processes, without requiring process modifications, would simplify the use of optics in computing. In particular, CMOS detectors would benefit optical interconnect receiver and optical clocking applications, where density, yield, uniformity, and low cost integration are desired. However, the PN junctions available for light detection in standard CMOS processes have a responsivity-speed tradeoff at 850 nm. This chapter presents experimental and simulation results on the characteristics of silicon detectors in commercial 0.25 μm bulk CMOS and 0.5 μm ultra-thin silicon-on-sapphire (SOS) processes. The use of shorter wavelength blue light is proposed to allow faster, more efficient carrier collection in CMOS detectors. Finally, low-jitter optical clocking of a digital circuit using blue light and SOS detectors is demonstrated experimentally.

## 5.1. Responsivity-Speed Tradeoff in CMOS Photo-detectors

It is clear from the previous chapters that, to achieve full swing optically injected clocks, on-chip low capacitance detectors with reasonably good response are needed. The detectors should be high-speed transit time-limited devices to achieve sharp rise and fall times, and they should be densely integrable to allow clock distribution to a number of injection points. One possibility for implementing dense low cost photo-detectors is to fabricate them in the CMOS process alongside the circuits. Achieving high speed, low capacitance and good response simultaneously in CMOS photo-detectors is challenging.

Silicon is a good material for photo-detection especially at visible wavelengths, but because its bandgap is ~ 1 eV, silicon is transparent at telecommunications wavelengths, and, because it is an indirect gap semiconductor, has a fairly long absorption depth of ~ 14 μm at 850 nm [1]. One constraint of the CMOS process is the relatively short depletion width of the available pn junctions. As shown in Fig. 5.1 (a) in a 0.25 μm CMOS process, light of wavelength 850 nm generates carriers deep into the substrate whereas the depletion regions are ~ 100 nm wide and ~ 100 nm from the surface. Only carriers generated near a depletion region experience an electric field and get collected quickly. A fraction of the remaining carriers diffuse upwards through the substrate and gradually get collected. This makes detectors in bulk CMOS slow, limiting their speed to kHz. Moreover, the excess substrate charge can diffuse into adjacent circuits. The speed problem can be fixed, but at the expense of responsivity. For example, silicon-on-insulator (SOI) CMOS processes have no substrate and therefore no carrier diffusion problem, as shown in Fig. 5.1 (b). SOI detectors achieve high-speeds at 850 nm but their responsivity suffers because so few carriers are generated.




(a) Bulk CMOS (b) SOI CMOS

Figure 5.1 Responsivity-speed tradeoff in bulk and SOI CMOS photo-detectors for 850 nm light Depletion regions are shown in gray

The promise of monolithic integration in CMOS has inspired many novel detector structures to mitigate the responsivity-speed tradeoff at 850 nm. The clever use of buried junctions in bulk CMOS achieved 1 Gb/s 850 nm detectors with a responsivity ~ 0.02 A/W [2]. Other novel detector structures have involved modifications to the CMOS process to enhance photo-detector performance. Among these are resonant cavity enhancement (RCE) detectors using distributed Bragg reflectors (DBRs) [3], transit-time limited metal-semiconductor-metal (MSMs) detectors on silicon-on-insulator (SOI) [4], roughened membrane MSMs [5], and grating coupled SOI waveguide detectors [6]. The fabrication of these detectors is compatible with CMOS but requires additional processing and integration. Within standard SOI processes, avalanche gain based detectors have been reported which require no additional steps but may need voltages beyond CMOS supply levels [7]. Trench PIN detectors [8] and thicker SOI materials have also been reported. These optimize the balance between speed and responsivity by maximizing the amount of silicon available for absorption at a given speed.

Detector capacitance is another important parameter for optical clocking and interconnects, because it directly impacts the required optical power, receiver bandwidth, voltage swing, and noise. Planar PIN detectors in SOI have smaller capacitance than deep trench or bulk detectors of similar active area. One interesting effect of an insulating substrate is that the capacitance of detectors in SOI can be very low for thin silicon layers. In this work, planar PIN detectors were fabricated in 100 nm thick silicon on sapphire having an estimated capacitance less than 5 fF for detectors as large as 30 x 30 $\mu m^2$. But, these thin silicon detectors have very poor response at 850 nm.

One way to improve the speed of CMOS photo-detectors without modifying their structure and without degrading the responsivity by two orders of magnitude is to not use 850 nm light but instead communicate using shorter wavelengths. For free space clock distribution there is flexibility in the optical wavelength that can be used. 850 nm light has been popular for short-haul optical links because of low fiber loss and the availability of low cost transmitters. Fiber loss is irrelevant for free space optics. A practical shorter wavelength for clocking may be 425 nm, obtained by frequency doubling existing 850 nm short pulse lasers. Fig. 5.2 shows that silicon has an absorption depth of ~ 135 nm in the blue ($\lambda$ = 420 nm). Therefore, at this wavelength more of the photo-generation would occur within the depletion region, making CMOS detectors potentially quite fast without as much of a responsivity tradeoff. Note that only 1-1/e (66 %) of the carriers are generated within one absorption depth, 86 % within two and nearly all within three. Thus, the most efficient SOI detector for blue light would have 400 nm (= 3x135) thick silicon. Alternately, 100 nm thick silicon would best absorb UV light of wavelength 255 nm. However, UV might be more easily absorbed in the dielectric layers above the detector.

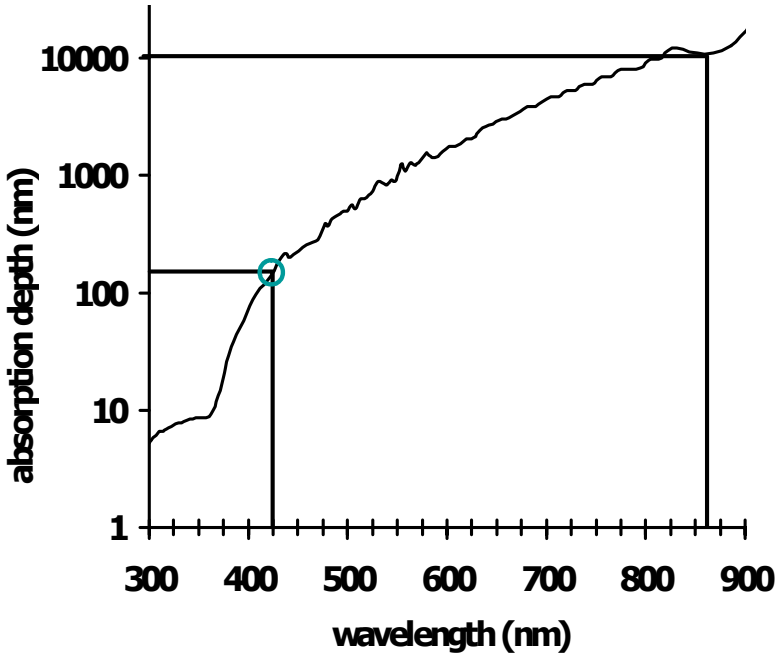



Figure 5.2 Absorption depth data for crystalline silicon vs. wavelength (adapted from S. Adachi [1])

One drawback of using shorter wavelength light is that each photon has more energy, but still creates only one electron-hole pair. As a result the amount of current generated per unit optical power is smaller with blue light than with red. The maximum possible responsivity in the ideal case where every photon creates η electron-hole pairs (η is the quantum efficiency) for 850 nm and 425 nm light is:

$$R = \frac{I}{P_{opt}} = \frac{\text{Generated Charge}}{\text{Incident Energy}} = \frac{q \cdot \eta \cdot N_{photons}}{N_{photons} \cdot h \cdot \nu} \qquad (5.1)$$

$$R = 0.68 \cdot \eta \ (850nm); \quad R = 0.34 \cdot \eta \ (425nm)$$

In a single pass device $\eta < 1$; the responsivity can be higher if the unabsorbed photons are reflected back to make multiple passes through the active region, in which case η can be larger than 1. Another potential drawback of using blue light to generate carriers close to the surface is that some carriers may not generate photo-current due to surface recombination, although the silicon-silicon dioxide interface has few recombination sites.

## 5.2. Comparison of Bulk and SOI CMOS Detectors – DC Responsivity and Capacitance

CMOS processes vary depending on the foundry and technology generation, but all are optimized for the fabrication of transistors. MOS transistors are made in islands of N and P doped regions called Nwells and Pwells inside which lie more heavily doped P+ and N+ diffusions that form the source and drain of the transistor. Hence, there are three different pn junctions available for photo-detection in any bulk CMOS process. Fig. 5.3 is a cross section of the 0.25 um twin well process used to fabricate the detectors in this work. Also shown are the three PN junctions A, B, and C. The drawing is not to scale.

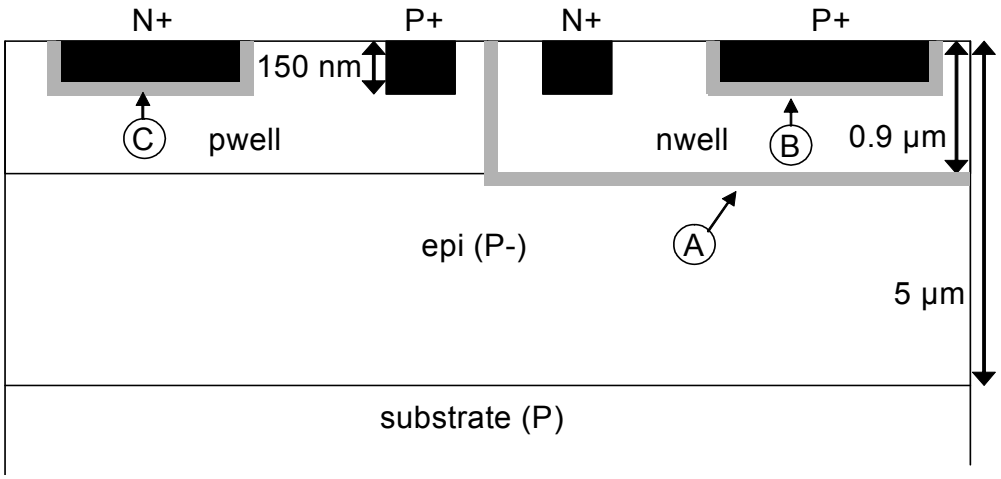



Figure 5.3 Schematic cross-section of photo-detectors in a bulk CMOS process. Junction areas are shown in gray and marked A, B, and C. Drawing is not to scale

The junction marked A utilizes the n-well and the lightly doped epi-silicon layer. Since the epi layer is lightly doped, this detector has the largest depletion width, and is expected to have the smallest capacitance of the three. Junction B utilizes the P+ region which would form the source/drain diffusion of a p-channel transistor, and the n-well. Similarly, junction C utilizes the N+ source/drain diffusion and the p-well. The diffusion

regions are degenerately doped and the well doping is moderately high so these junctions are expected to have fairly high capacitance. A differential optical scheme like the receiver-less scheme requires two reverse biased photo-detectors to be connected in series. For proper function, this requires two detectors with similar responsivities and similar capacitance, at least one of which should have a P-region that is not connected to ground. Junctions B and C are the closest to fulfilling this requirement, but note that junction B cannot be fabricated separately from junction A, so a P+Nwell photo-detector necessarily has beneath it an Nwell-Pepi junction. In measurements involving this detector the Nwell is connected to Vdd and the substrate is always grounded as is necessary in CMOS processes.

The DC responsivity of the N+Pwell and P+Nwell detectors was measured using blue light generated by frequency doubling a short pulse Ti:sapphire laser with center wavelength 830 nm and pulse-width 6.5 nm. The 415 nm blue beam was separated from the residual 830 nm beam using wavelength selective mirrors. For responsivity measurements, the amount of blue light incident on the CMOS detectors was measured using a calibrated commercial GaP photo-detector[1]. Table 5.1 lists the DC responsivities of the detectors in the blue. The I-V characteristic for the detectors was normal and is included in Appendix 5.1. The dark current of the detectors was measured to be 3 - 5 nA. The measured DC responsivities are lower than the 0.34 A/W theoretical maximum from equation (5.1) implying an external quantum efficiency $\eta$ of ~ 20 %. Possible sources of loss could be reflection or absorption by the dielectric layers above the silicon. The dielectric stack could not be modeled here as its composition was not public. Carriers

[1] GaP photo-detectors are sensitive to blue light but are not sensitive to infrared light.

may also have been lost to surface recombination or recombination in the bulk. The DC responsivity at 850 nm for the N+Pwell detector was less than that for 425 nm as expected, because some of the deep carriers generated by 850 nm light would recombine in the bulk, and not all would diffuse up towards the depletion region.

Table 5.1 Measured blue responsivity and capacitance for bulk CMOS photo-detectors

| | Responsivity A / W (blue) | Responsivity A / W (850 nm) | Capacitance (fF) Area: 10x10 $\mu m^2$ |
|---|---|---|---|
| N+Pwell | 0.064 | < 0.025 | 119 |
| P+Nwell | 0.08 | | 103 |

The capacitance of each detector is also listed in Table 5.1 and was measured using on-chip inverter-based ring oscillators. Each node of the oscillator was loaded with the detector and the resulting oscillation frequency was divided down and measured on an RF spectrum analyzer. Separately, a plot of ring oscillator frequencies as a function of load capacitance was generated using SPICE simulations. Measured frequencies were compared to simulations to determine the capacitance of the detectors. For comparison, the Nwell-Pepi detector had a capacitance of 18 fF for the same area. As expected the N+Pwell and P+Nwell detectors have higher capacitance due to the thin depletion widths.

The SOI CMOS photo-detectors studied here were fabricated by Peregrine Semiconductor in their commercial 0.5 μm silicon-on-sapphire process. The silicon in this process was 100 nm thick, and an intrinsic silicon layer was available. This allowed multi-fingered lateral P-I-N structures with any length of intrinsic silicon between heavily doped N and P regions as shown in Fig. 5.4. The metal fingers drawn in dark color have alternating polarity and are reflective. As such the active area of this detector is somewhat smaller than its physical area. Note that there is no substrate terminal to be

connected to ground, and that these detectors are symmetric and can easily be connected in a differential series totem-pole. The material between the fingers is intrinsic silicon and its width (minus a ~ 0.1 μm spacer on each side) defines the finger-spacing of the detector. The figure shows a two finger lateral P-I-N detector of 6 μm finger spacing. Here the DC responsivity for a 6 μm and a 2.4 μm spacing detector was measured.

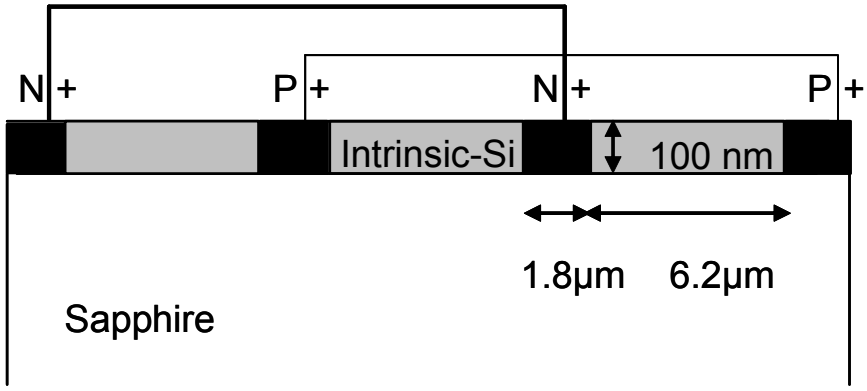



Figure 5.4 Schematic cross-section of a two finger lateral P-I-N SOI photo-detector

Table 5.2 lists the measured responsivity and calculated capacitance for the two SOI detectors. The blue responsivity was measured on large 100 x 100 $\mu m^2$ photo-detectors onto which a 60 μm diameter spot of blue light was focused, again using frequency doubling of the short pulse Ti:sapphire laser. I-V curves were measured for various power levels and are included in Appendix 5.1. The detector response for both 2.4 μm and 6 μm spacing detectors was found to increase with applied bias. The responsivity in Table 5.2 was at a bias of 3.0 V. At the maximum tested voltage of 6 V, the 6 μm spacing detector had a responsivity of 0.052 A/W. The responsivity at 850 nm was measured similarly and the corresponding I-V curves are also included in Appendix 5.1. The data indicate a 50X improvement in photo-generated current by the use of blue light. Finally, the capacitance was calculated using a model for the fringing fields in a metal-

semiconductor-metal structure using sapphire as the substrate [9]. Note that the values listed in Table 5.2 are for a detector of size 25 x 30 $\mu m^2$. The theoretical capacitance of a 10 x 10 $\mu m^2$ detector is < 1 fF. SOI detectors have lower capacitance than detectors in the bulk process because in the SOI case the junction towards the substrate is absent.

Table 5.2 Measured responsivity and calculated capacitance for planar P-I-N SOI photo-detectors

| | Responsivity A / W (blue) | Responsivity A / W (850 nm) | Capacitance (fF) Area: 25x30 $\mu m^2$ |
|---|---|---|---|
| 2.4 μm P-I-N | 0.043 | 0.00092 | 4.9 |
| 6 μm P-I-N | 0.038 | | 1.8 |

The expected responsivity from these SOI detectors was less than the theoretical maximum of 0.34 A/W. As noted in section 5.1, the absorption depth of silicon in the blue was 135 nm whereas the thickness of silicon in these SOI detectors was 100 nm. Thus only 52 % of the light incident on the active area would generate carriers. Secondly, the metal fingers of the device were reflective so that of the incident optical power only 55 % and 70 % fell on active areas for the 2.4 μm and 6 μm detectors respectively. Thus the highest expected responsivities from these detectors were 0.097 A/W and 0.12 A/W for the 2.4 μm and 6 μm devices. The quantum efficiencies η were therefore 50 % and 30 % respectively. The dielectric stack thickness and composition was also not available but was modeled approximately from the available data. The model results, which include potential cavity resonance effects and Fresnel reflections, are included in Appendix 5.1. The model suggests a further 20 % loss was possible[2], which would lower the estimates to 0.077 A/W and 0.096 A/W. However, the model was quite sensitive to dielectric

[2] Note that due to cavity enhancement the loss is lower than that due to simple fresnel reflection.

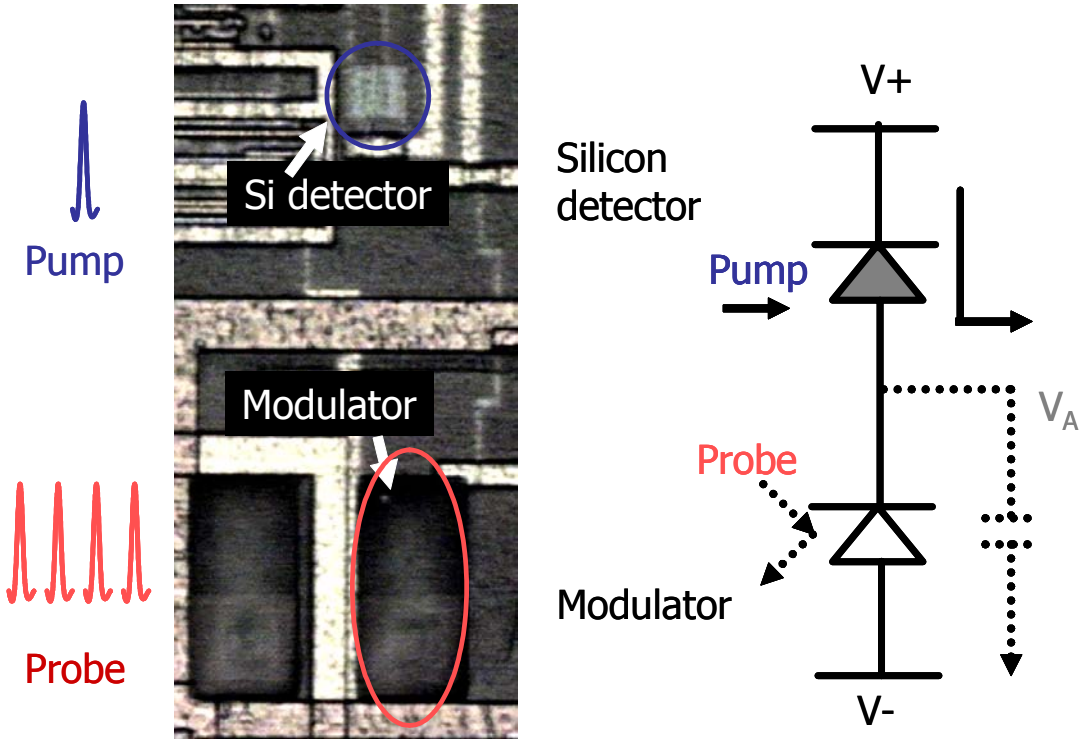
thickness and composition which were known only approximately for this technology. The data in figure 5.15 of the Appendix assumes two dielectric layers of thickness 0.7 μm and 6.2 μm with dielectric constants 7.5 and 3.9 for passivation and oxide respectively. However, even a change of 0.1 μm in the thickness of the passivation changes the effective transmission characteristics. Hence, this remains a potential source of detector response degradation.

The data suggest that the rate of recombination inside the SOI detectors was greater than would be expected for intrinsic silicon. A possible cause would be the presence of ionized traps inside the material or at the silicon-sapphire interface. Information about the trap densities was not available from the foundry; however, the carrier lifetime had been measured by them to be ~ 5 ns. Also I-V curves in Appendix 5.1 show a voltage dependent responsivity, which might indicate a non-intrinsic material. A high density of traps could also make it difficult to deplete the detectors. The detector structure was simulated in MEDICI using carrier lifetimes in the range of 100 ps to 5 ns and doping densities ranging from 1e13 $cm^{-3}$ to 3e16 $cm^{-3}$. A 1 ns lifetime and a doping of 1e14 $cm^{-3}$ best matched both the optical response and the I-V characteristics. However surface recombination at the silicon-sapphire surface was not modeled in MEDICI.

## 5.3. Measurement and Simulation of SOI CMOS Detector Speed with Blue Light

The speed of the SOI detectors was characterized in a pump-probe experiment. A blue light pulse-train (pump beam) was generated by frequency doubling a 160 fs pulse-width mode-locked Ti:sapphire laser centered at 845 nm in a 1 mm thick BBO crystal. A total of 20 mW of average blue power was available for experiments, in pulses ~ 12ns apart. A

dichroic beam-splitter separated the two wavelengths after the conversion. The blue pulse train (pump beam) was focused onto the SOI CMOS photo-detector. Part of the remaining unconverted 850 nm pulse-train was used as the probe beam for modulators which measured the electrical response of the circuit. The SOI CMOS chips were integrated with electro-absorption modulators via flip-chip bonding to enable optical characterization of the temporal response of the silicon detectors to blue light.




(a) (b)

Figure 5.5 (a) Flip-chip bonded GaAs-AlGaAs MQW devices with SOI CMOS detectors. The probe delay is swept. (b) Schematic of detector-modulator connection

Fig. 5.5 (a) is a top-view microscope picture of the integrated modulators and SOI CMOS detectors. As described in the previous chapter, the modulators were molecular beam epitaxy (MBE) grown GaAs-AlGaAs multiple-quantum-well (MQW) P-I-N diodes based on the quantum-confined Stark effect (QCSE) [10]. The QCSE leads to the

absorption of this device being voltage dependent. For the modulators used here, a beam of wavelength 845 nm would be absorbed progressively less as the voltage across the modulator increased. The probe wavelength was chosen to be 845 nm because the modulator's absorption change was monotonic at this wavelength; however, the contrast ratio was low with only 8 % intensity variation over the range of voltages used. As a result, a high probe power (~ 300 μW) and also a high pump power (~ 10 mW) were used.

The modulators were connected to the SOI detectors as shown in Fig. 5.5 (b). Fixing the voltage on the p-side of the modulator and measuring the intensity of the reflected light from it, produced a signal that was proportional to the voltage on the n-side, which was connected to the detector. As shown in Fig. 5.5 (b) the 425 nm pulse-train (pump) on the detector raised the voltage on the modulator. The pulse-train on the modulator (probe) was delayed relative to the pump using a corner-cube reflector on a computer-controlled delay stage. As the delay of the probe pulse-train was swept, the voltage rise caused by the CMOS detector was mapped out via the QCSE. Using a polarizing beam-splitter and a quarter wave plate, reflected probe light from the modulator was deflected to a fiber-coupled commercial photo-detector and measured on a lock-in amplifier. A chopper in the path of the pump pulse-train modulated the beam at the frequency detected by the lock-in amplifier. Fig. 5.6 shows the experimental set-up.

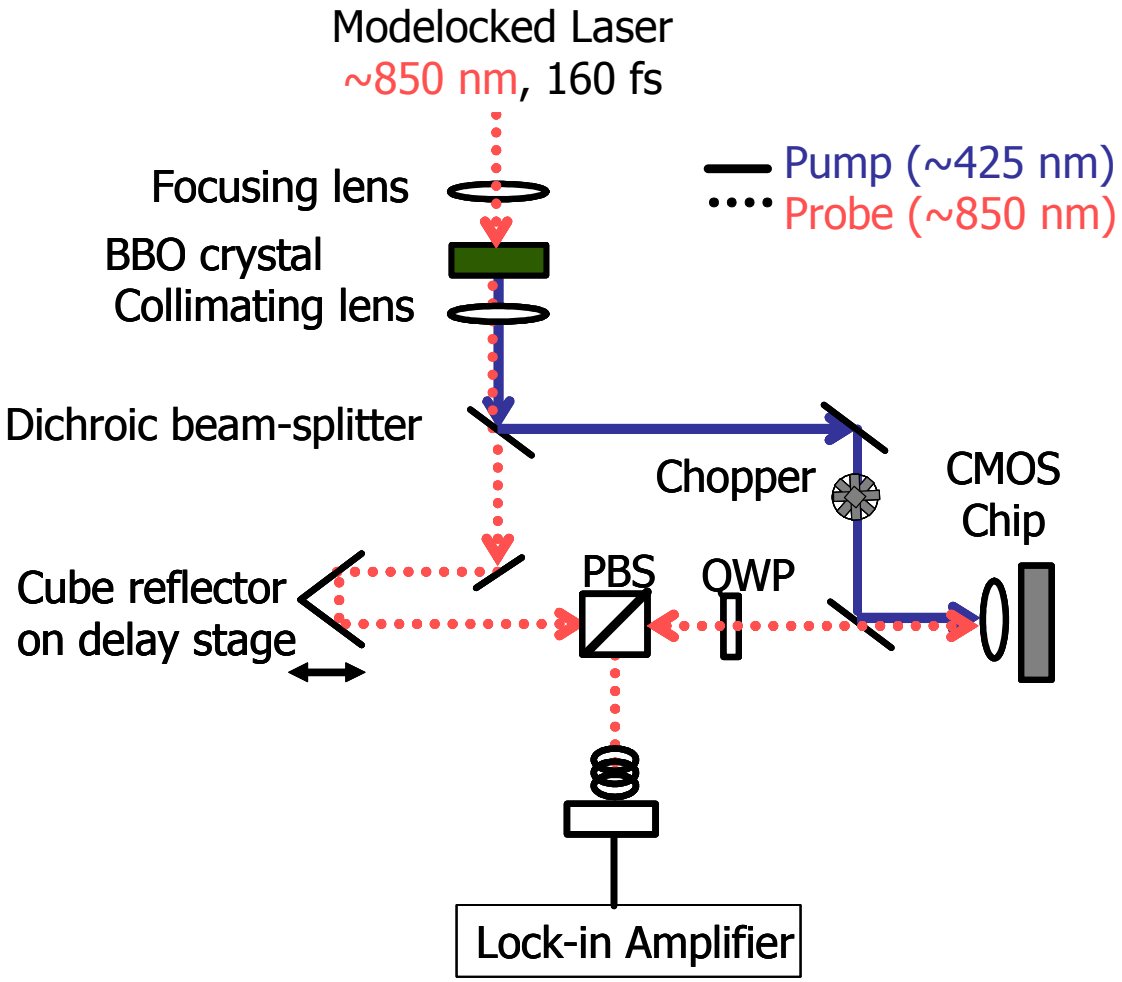



Figure 5.6 Experimental set up for pump-probe measurement

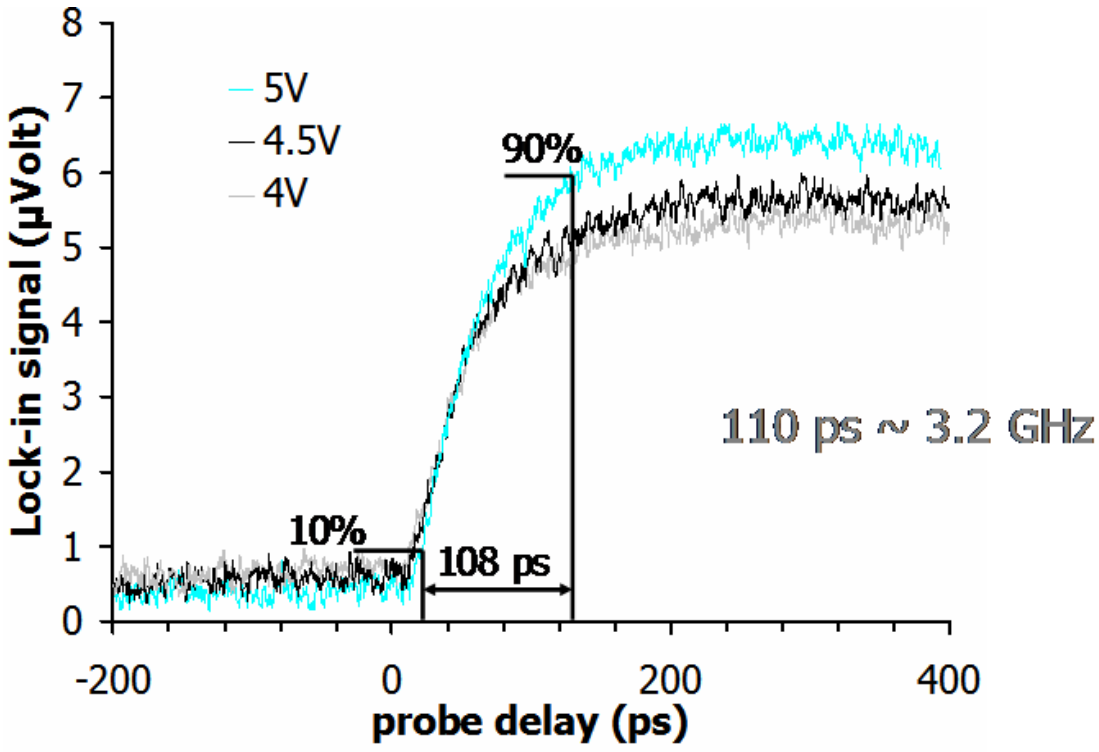



Figure 5.7 Pump-probe measurements of the rise time of a 6 μm finger spacing planar P-I-N SOI detector for 4, 4.5, and 5 V bias

Fig. 5.7 is a plot of the reading from the lock-in as a function of relative delay between pump and probe. At ~ 0 ps the pump pulse arrived. As the voltage on the modulator rose, its absorption decreased leading to a rise in the lock-in signal. Sweeping the arrival time of the probe with respect to the pump mapped the voltage rise caused by the CMOS photo-detector with picosecond precision. Fig. 5.7 shows the signal for three different biases. This voltage remained high until sufficient pull-down current from the modulator swept out the charge and restored the node to the negative supply. The pump and probe beam powers were the same for the three curves. The signal swing increased with voltage. The increase was not expected to be exactly proportional to the voltage as the modulators were not linear over all voltage ranges. Independent modulator contrast ratio measurements indicated that the total signal swing in Fig. 5.7 corresponds to a ~ 4V rise

in the voltage. Focusing an additional pull-down CW beam on the modulator for additional pull-down did not decrease the reset voltage, indicating the node was swinging fully to the negative supply.

The 10 % - 90 % rise times for the three curves were: 104, 107 and 113 ps respectively for the 4, 4.5 and 5 V biases. The detector finger spacing was 6 μm, thus for a 4.5 V bias the corresponding field was 0.75 V/μm. The drift velocity of holes in silicon at 0.75 V/μm is ~ 2.5 x $10^6$ cm/s, while that of electrons is ~ 7.5 x $10^6$ cm/s [11]. Thus the expected full swing rise time for a transit-time limited detector was between 80 - 250 ps, with the 10 % - 90 % rise time being slightly less. The data agree with this rough transit time estimate. Additionally MEDICI simulations of the speed of a 6 μm finger spacing photo-detector were carried out. Again no surface recombination or trap density was simulated and the active region was assumed to be 1e14 $cm^{-3}$ while the N and P regions were heavily doped (1e20 $cm^{-3}$). In the simulation a 425 nm short pulse optical input impinged on the detector at time zero. The integrated photocurrent or, equivalently, the total charge collected at the detector terminal was plotted as a function of time, as shown in Fig. 5.8 for 6 μm and 1.2 μm finger spacing P-I-N SOI detectors. The simulated 10 % - 90 % rise time was 120 ps for the 6 μm detector which corresponds to 3 GHz bandwidth. The 1.2 μm detector simulation gave a 15 ps rise time implying 20 GHz potential bandwidth. However, because of the unknown trap density and the use of a high optical power in this measurement, the data and simulation which are mutually consistent represent the behavior of the detector under high power only.

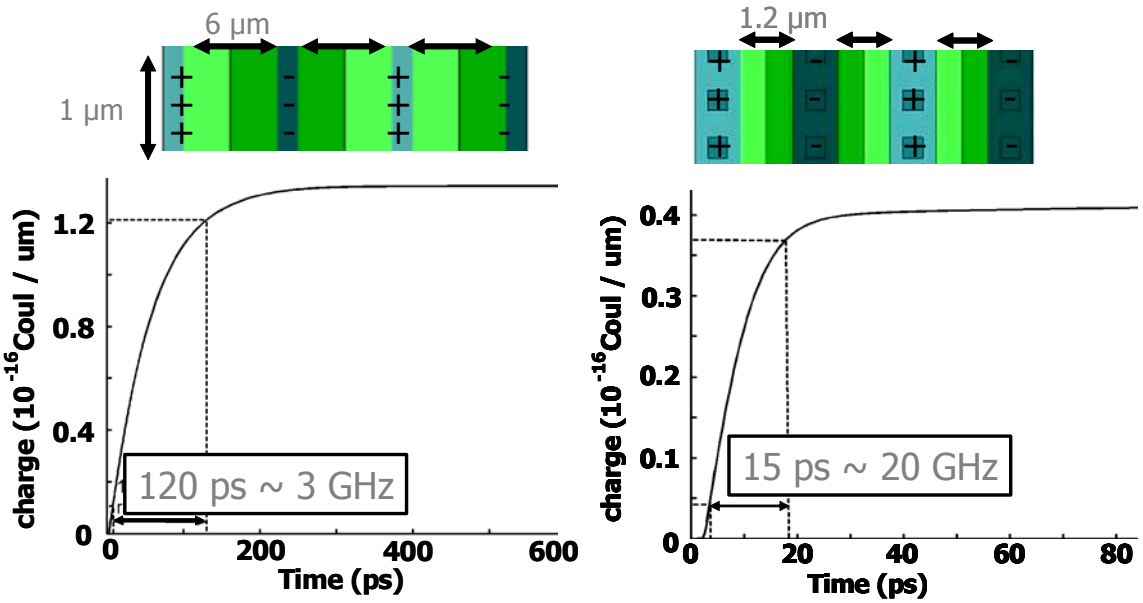



Figure 5.8 MEDICI simulations of the integrated photocurrent vs. time for planar p-i-n SOI detectors with 5 V bias for 6 µm and, in the inset, 1.2 µm finger spacing

## 5.4. Optical Clocking of a Digital Circuit using SOI CMOS Detectors and Blue Light

A series totem-pole of two identical SOI detectors was used to inject an optical clock to the PRBS circuit described in chapter 4. The experimental set up and measurement apparatus were identical to those used in the experiment in chapter 4. The only difference apart from the detectors and the laser wavelength was the optics, such as lenses and beam splitters, which were coated for blue light. Fig. 5.9 shows a microscope photograph of the detectors connected to the PRBS and a schematic of some of the optical set up. The load capacitance for the clock input was the two detectors, a total of 200 µm of wire and 20 fF of buffer input capacitance. The estimated total load was ~ 35 fF. The total bias, which fell across the series combination of the detectors, was 3.3V. At 80 MHz (12.4 ns) therefore, the required photo-current per detector was expected to be ~ 10 µA. The

responsivity of the SOI diodes was known to be voltage dependent, thus if a lower bound of 0.01 A/W is assumed, the amount of optical power required for the experiment should have been ~ 1 mW per beam.

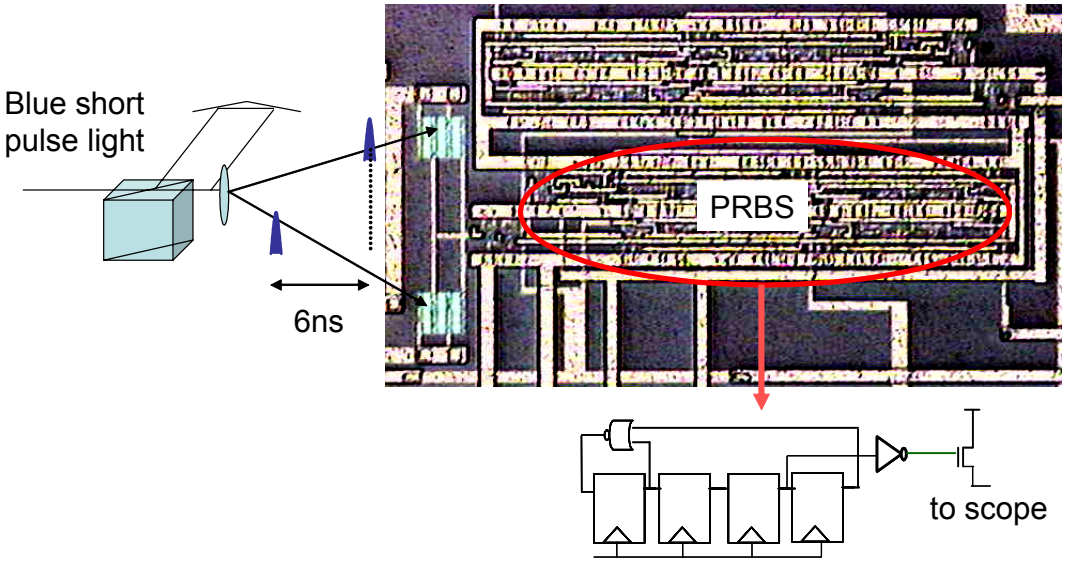



Figure 5.9 Experiment for optical clock injection to digital PRBS using blue light and SOI CMOS photo-detectors

The actual experiment required more optical power than expected. After 500 µW of blue power was focused onto the photo-detectors, the PRBS did not immediately begin to function. When Vdd was lowered to ~ 0.8 V the PRBS began to work, however the jitter on the output was ~ 12 ps rms. With 2 mW power in each beam, it was possible to raise Vdd to 3.3 V and obtain 4 ps rms jitter. This was not necessarily the lowest optical power at which the PRBS functioned this well. However, it was difficult to find the lowest power because the pull up and pull down beams needed to be re-balanced each time either one was disturbed. The lowest jitter achieved was 1.5 ps rms as shown in Fig. 5.10. The best jitter performance was obtained by overdriving the detectors with 5 mW of optical power per beam.

Compared to the result for GaAs photo-detectors in chapter 4, which was 3 ps rms jitter, the above 1.5 ps rms is superior. It is possible that the larger than expected optical power was necessary to obtain sharper rise times and thus lower jitter. The high optical power would have created a large number of carriers inside the detector. If the detector were filled with charge then a small displacement of that charge could produce sufficient voltage swing. That is, a complete movement of charge from one electrode to the other would not be required to produce a full swing voltage, thereby making the detector react faster. A sharper rise time at the clock input could have lowered the jitter.

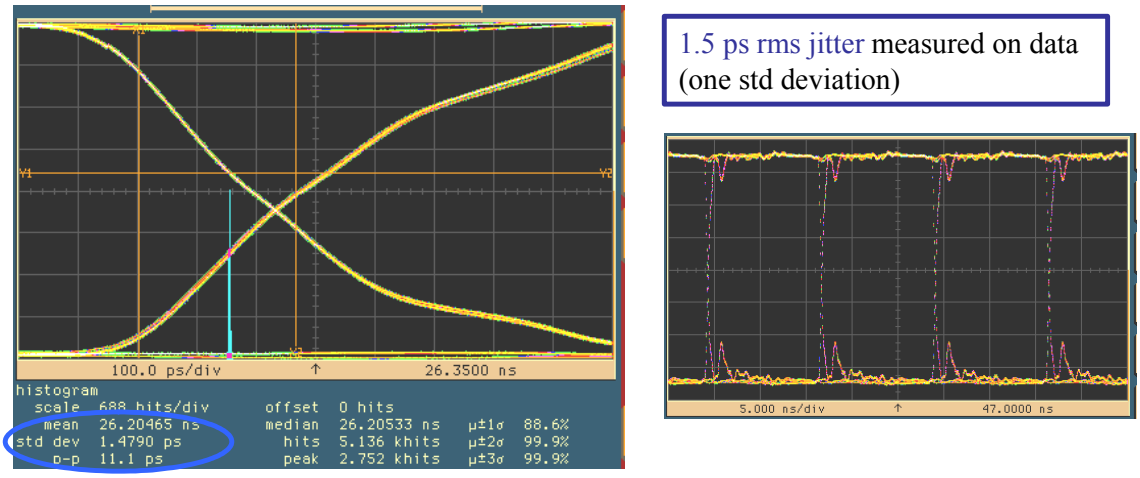



Figure 5.10 Zoomed-in picture of eye diagram of PRBS output when the PRBS is optically clocked using SOI CMOS photo-detectors and blue light. The histogram of the jitter on the falling edge is shown. A zoomed out version is also shown

In conclusion, this work is apparently the first to investigate the use of blue short pulses for high speed CMOS photo-detectors. As a first step, the DC responsivities in the blue for some basic photo-detectors in bulk CMOS and an SOI process were characterized. While relative to the 850 nm case a responsivity improvement of ~ 50X was measured for the SOI detectors, overall the responsivities were lower than calculated. The data suggest that monolithic CMOS detectors in the bulk and SOI processes used

here have a greater recombination rate than expected. Perhaps surface recombination is more important in the blue than at longer wavelengths. It is also possible that CMOS passivation and dielectric layers reflect or absorb blue light. Although further work is required to investigate these and other possibilities, functional optical clocking was demonstrated using blue light and monolithic SOI photo-detectors.

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# APPENDIX 5.1 Measured I-V Characteristics of CMOS Detectors and Transfer Matrix Simulation of the Effects of Passivation

Figure 5.11 I-V curve for P+Nwell and N+Pwell bulk CMOS detectors with ~ 425 nm short pulses

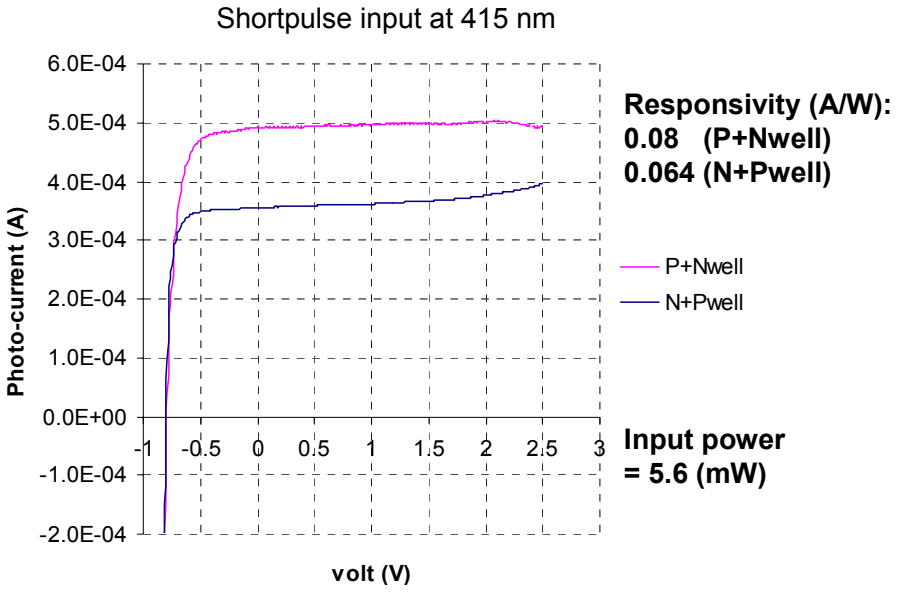



Figure 5.12 I-V curves for 2.4 μm spacing SOI detector with ~ 850 nm short pulse light

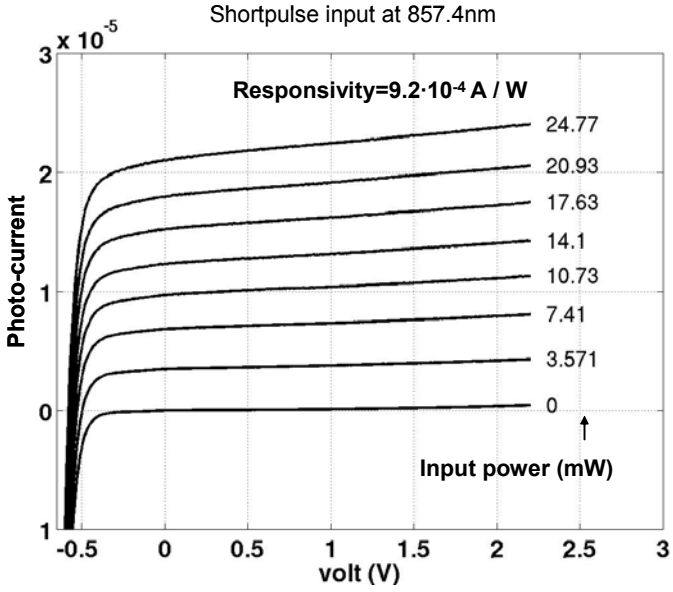


Figure 5.13 I-V curves for 2.4 μm spacing SOI detector with ~ 425 nm short pulse light

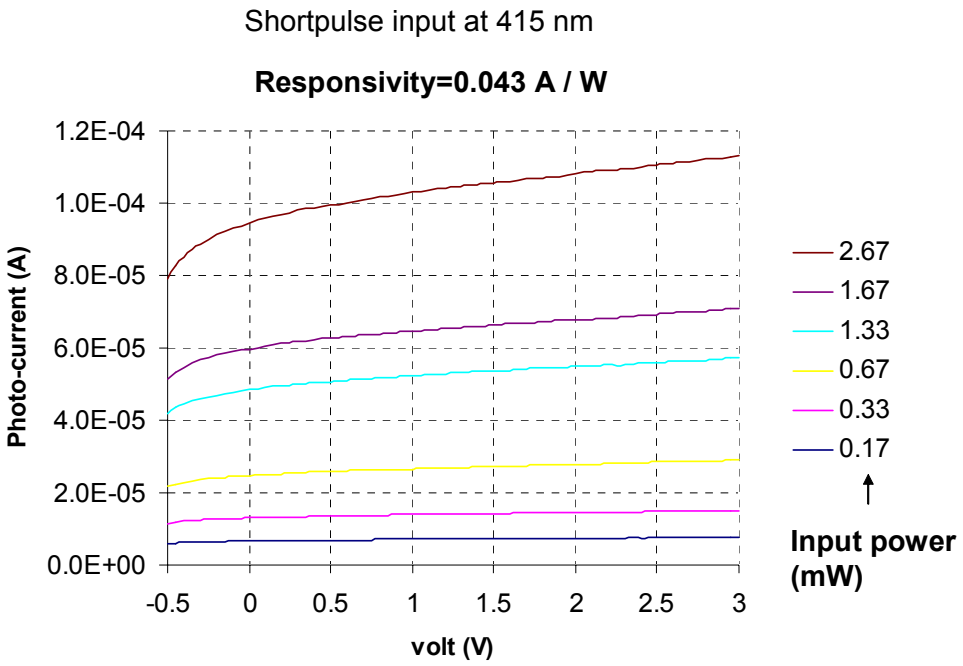



Figure 5.14 I-V curves for 6 μm spacing SOI detector with ~ 425 nm short pulse light

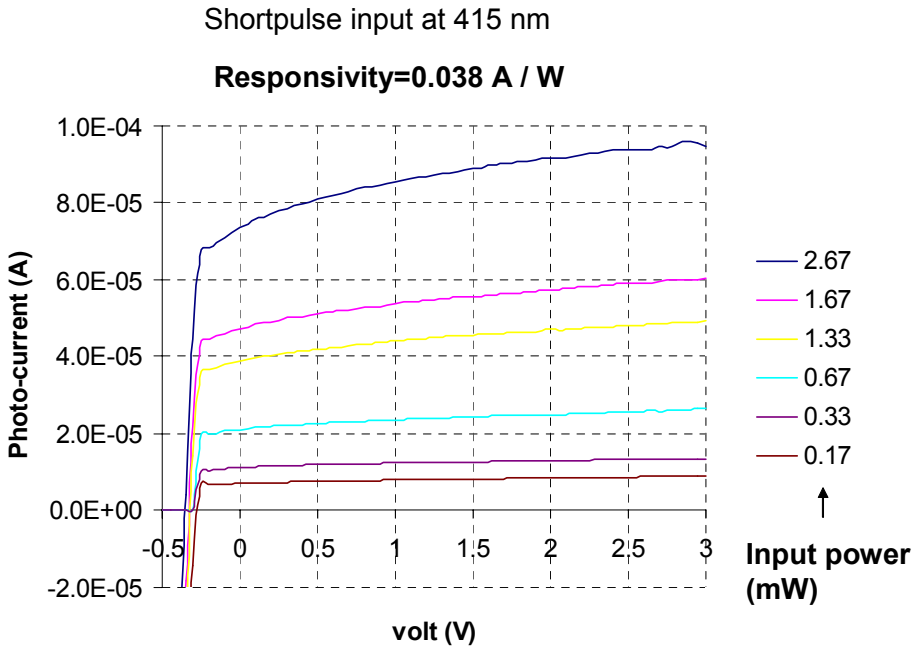
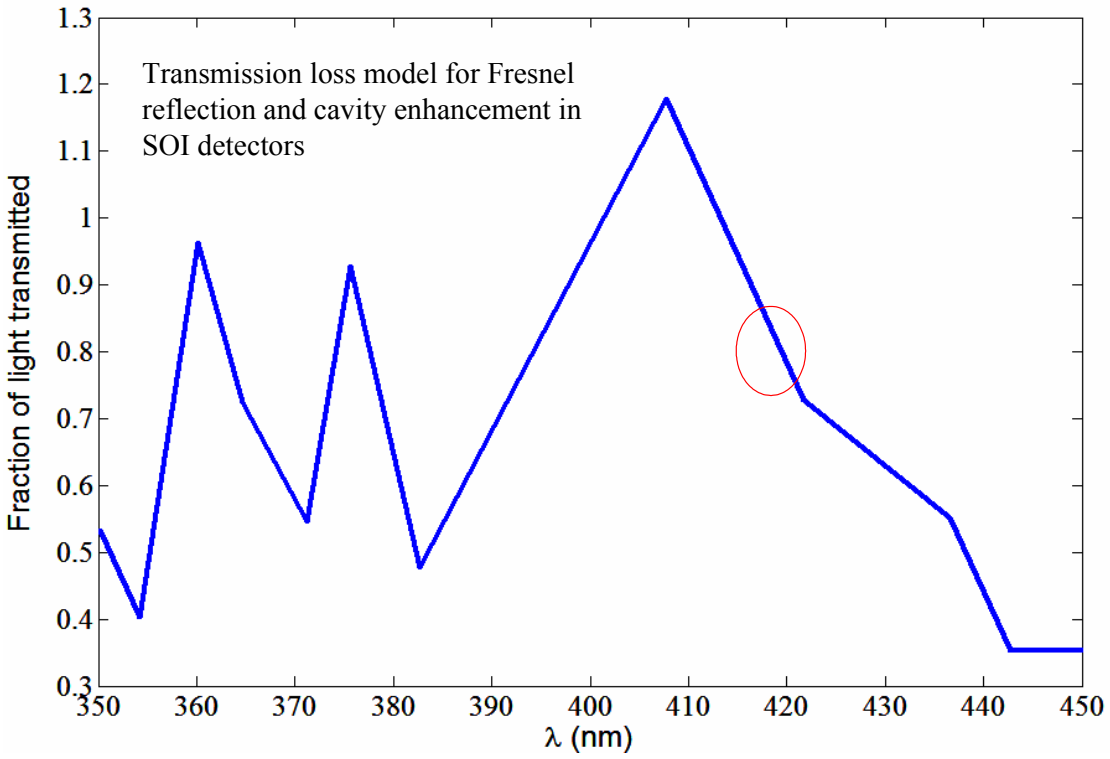


Figure 5.15 Results of transfer matrix model for Fresnel reflection losses and cavity effects in the SOI detectors; red circle shows the wavelength range of interest in the experiment
(note that the graph is discontinuous because the absorption depth vs. wavelength data for silicon is discrete)



# Chapter 6

# Optical Clock Distribution for Optical Links

Experiments in the previous two chapters have involved optical clock injection to a single injection point using two different detector integration schemes. This chapter describes a clock distribution experiment for interconnect or link applications. A communication link consists of a transmitter, a channel and a receiver. The transmitter and receiver each have a clock or set of shifted clocks which define the boundaries of the bits. The precision, speed, and synchronicity of the transmitter and receiver clocks affect the speed, error rate and power consumption of the link. Here the distribution of a multiphase optical clock to the transmitter half of an optical link will be described. This experiment shows low jitter, multiphase optical clock distribution to four points with precise but mechanically adjusted skew tuning.

## 6.1. Motivation for Optical Clocking in Links

Semiconductor scaling allows CMOS chips to run faster and process a greater quantity of information with each new generation. This creates demand for even greater off-chip bandwidth for communication between chips as implied by Rent's rule [1]. Chip size is projected to stay fairly constant despite speed scaling. As a result the density of off-chip wiring cannot increase much. Thus, either existing off-chip wires must be engineered to communicate faster or an alternate high bandwidth interconnect technology must be used. In either case, the interconnect data rate per line is higher than the on-chip clock frequency for critical off-chip interconnects. Therefore, time division (de)multiplexing is used for (de)serializing data from the chip [2]. For example, a 10 Gb/s off-chip data rate can be achieved with a 2.5 GHz internal clock by multiplexing four bit streams at the lower rate onto one high-speed link using a four phase shifted clock as shown in Fig. 6.1, for an optical link. An identical (phase locked) clock is needed at both the transmitting and receiving chips. The timing accuracy of the shifted clocks directly affects the maximum bit rate of the link.

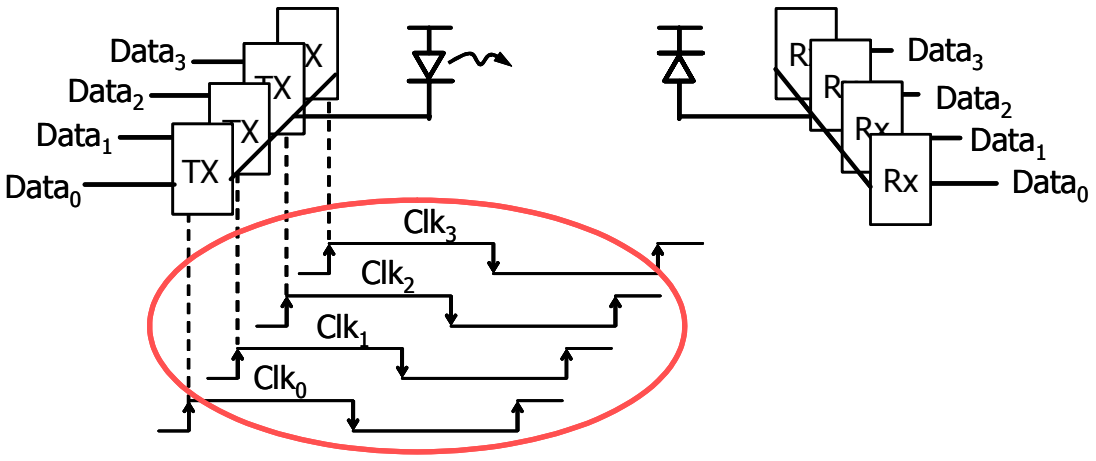



Figure 6.1 Optical link with four phase multiplexed clocking

The generation and distribution of precise multiphase GHz electrical clocks is a challenging task for three reasons. First, the design of CMOS oscillators which produce multi-GHz clocks with the required phase stability (typically << 10 % of clock frequency) is difficult [3-6]. Second, the wires in the on-chip and off-chip distributions introduce skew making it necessary to use active tuning and clock recovery for precise phase alignment. Third, buffering and distribution of clock phases significantly increases the total electrical power consumption.

The optical clock can be distributed with low loss and better than 1 % uniformity in optical power, and since air is not lossy or dispersive like wire, the same clock can be delivered to the transmitter and receiver without relative skew between the two. Moreover, the phase of each distributed clock can be set very precisely using optical path delays. Since the speed of light in air is ~ 300 μm/ps, and μm length adjustments are easily implemented with a motorized stage, sub-picosecond phase adjustment can be achieved. One drawback of optical clocking however is that generally the frequency and phase tuning mechanisms are slow. Also it requires integrated optical devices, and stable optical alignment.

Optical clocking becomes particularly attractive for links when the links themselves are optical, because then the overhead for adding an optical clock is minimized. An optical link consists of a laser or modulator driven by a CMOS circuit on the transmitting chip, and a photo-detector integrated with a CMOS receiver on the receiving chip. Optical links are currently used for board-to-board and longer interconnects, while copper wire dominates high speed chip-to-chip interconnections. However, as off-chip data rates exceed 10 Gb/s the power consumption and complexity of equalization and crosstalk

management for wires might make an inherently high bandwidth interconnect technology more mainstream. The optical alternative has many advantages as discussed elsewhere [7-10] and also enables new approaches such as WDM and TDM [11].

## 6.2. Experimental Approach

A test chip, shown in Fig. 6.2, was fabricated in a 0.25 µm standard CMOS process to display the potential for using mode-locked lasers and receiver-less detection to generate multiple phase clocks for use in serial link applications. The chip includes clock phase multiplexers to provide an electrical output for measuring jitter and phase spacing/resolution of the optical clocks. To enable a comparison of optical and electrical clocking for links, the chip was a modified version of a previous chip which successfully demonstrated a full optical link with five-phase electrical clocking [12]. The modified version was re-designed for a four phase optical clock by Samuel Palermo and Azita Emami-Neyestanak under the supervision of Prof. Mark A. Horowitz.

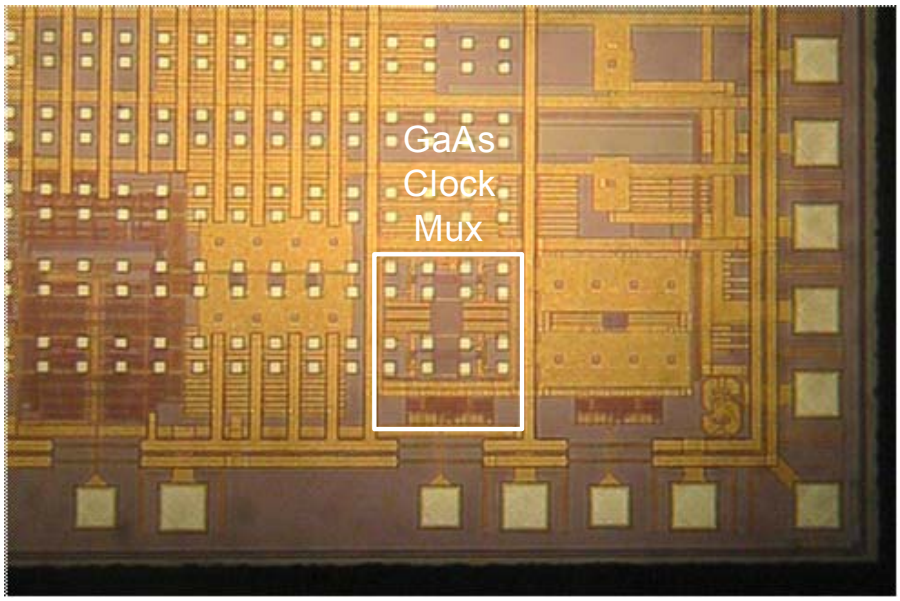



Figure 6.2 Optical clock-distribution for interconnects - test chip micrograph

In an optical experiment, four clock phases, nominally spaced at 200 ps, were brought onto photodiodes in a receiver-less configuration. In general, such diodes can be integrated on the chip, though for these experiments, commercial GaAs PIN detectors wire-bonded to the CMOS chip were driven with 850 nm short pulse light. Fig. 6.3 shows the laboratory optical setup used in these experiments. The optics shown generates four pairs of light beams using a beam splitter and two corner cube reflectors (marked cc in Fig. 6.3) which were mounted on micrometer translation stages. The relative timing of the clock pulses is set by the position of the reflectors, noting that 300 microns of propagation distance in free space corresponds to 1 ps of optical delay.

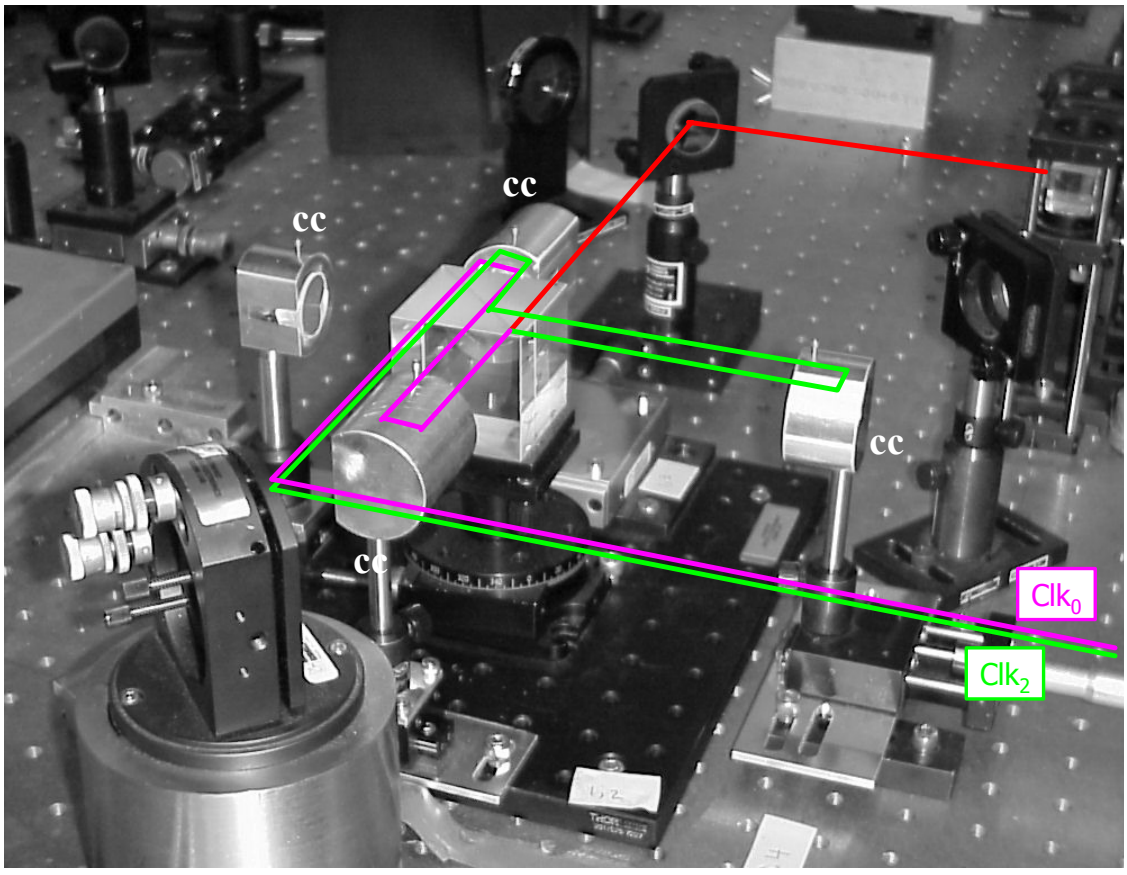



Figure 6.3 Optical setup for 4-phase clock spacing and distribution. Two beams shown for simplicity. The four corner cube (CC) reflectors are marked

The four clocks are then individually selected through a mux to drive the output stage in order to measure jitter and phase spacing over a common electrical channel. The measurement circuit is exactly the same as it was for the electrically clocked optical link chip. Fig. 6.4 a) shows the electrical clock distribution and measurement circuit for the previous chip where a clean off-chip reference clock was used to trigger an on-chip 5-stage ring oscillator PLL which provided five clock phases to the receiver and transmitter and also to a mux through which the clock itself was monitored. Fig. 6.4 b) shows the receiver-less four phase optical clock distribution and measurement circuit used here.

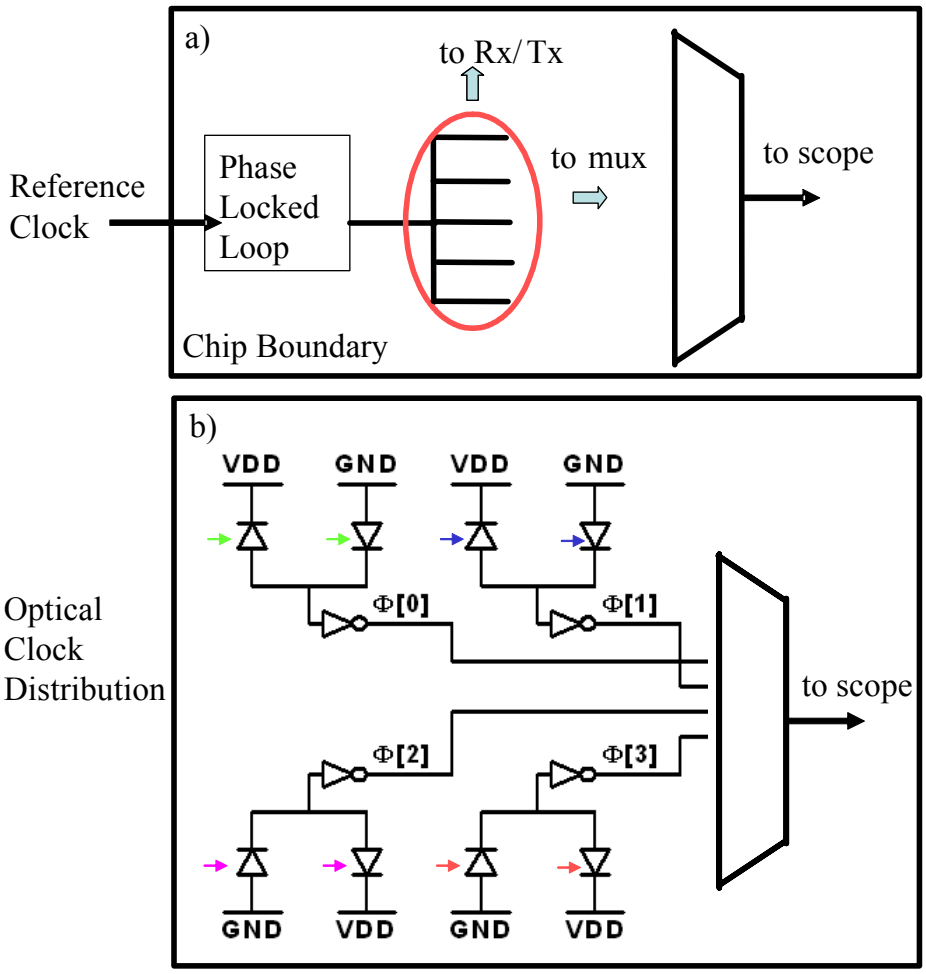



Figure 6.4 a) Electrical clock distribution for an optical link chip b) Optical clock distribution with receiver-less clocking. Different timing of the optical pulse pairs' arrival at the photodiodes leads to the controllable generation of the clocks with different phases, $\phi[1]$ to $\phi[4]$

## 6.3. Multiphase Optical Clock Distribution Results

In these experiments, the optical clock, monitored on a digital channel analyzer/scope via the mux, produced an output clock signal with 0.93 ps rms jitter as shown in Fig. 6.5. Fig. 6.6 shows two adjacent phases tuned to a nominal spacing of 200 ps. For comparison, the electrical clocks generated from the supply-regulated 5-stage ring-oscillator PLL in the same 0.25 µm technology, when driven by a high-performance off-chip pulse generator, had 1.74 ps rms jitter, and peak-to-peak phase variation of 11.3 ps between the 5 electrical clock phases.

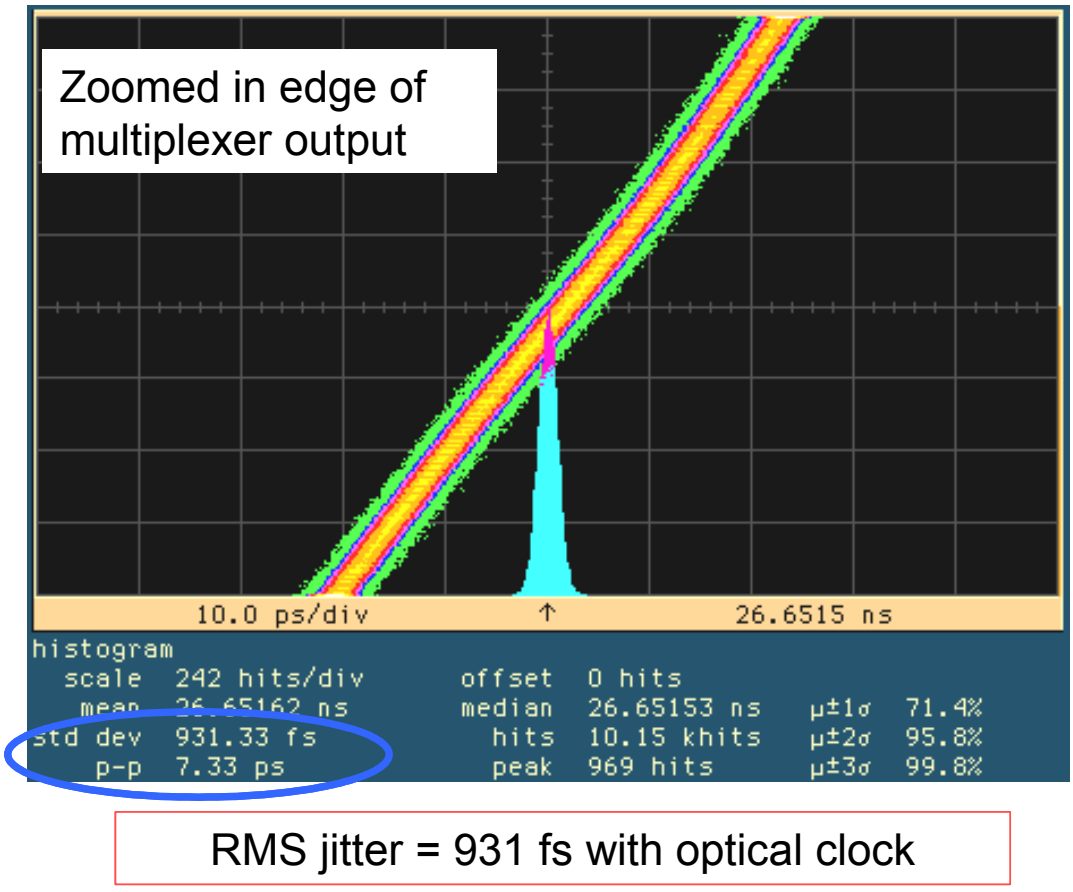



Figure 6.5 Jitter histogram for optically-triggered electrical clock output - GaAs PIN detectors driven with 850nm light

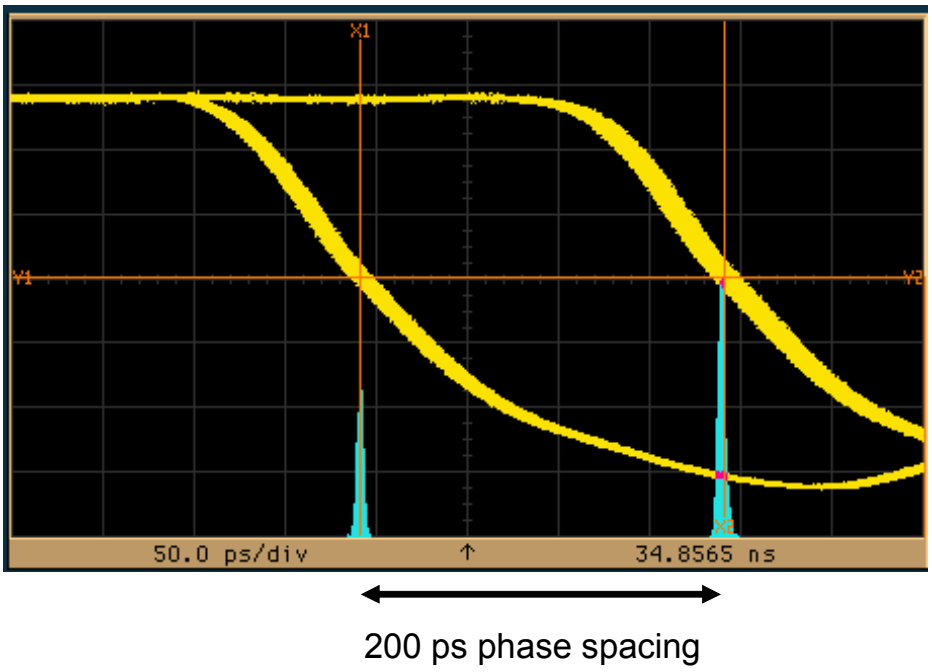



Figure 6.6 Overlay of two clock phases of the optical clock distribution showing a phase spacing of 200 ps, which was tunable over a 160 ps range

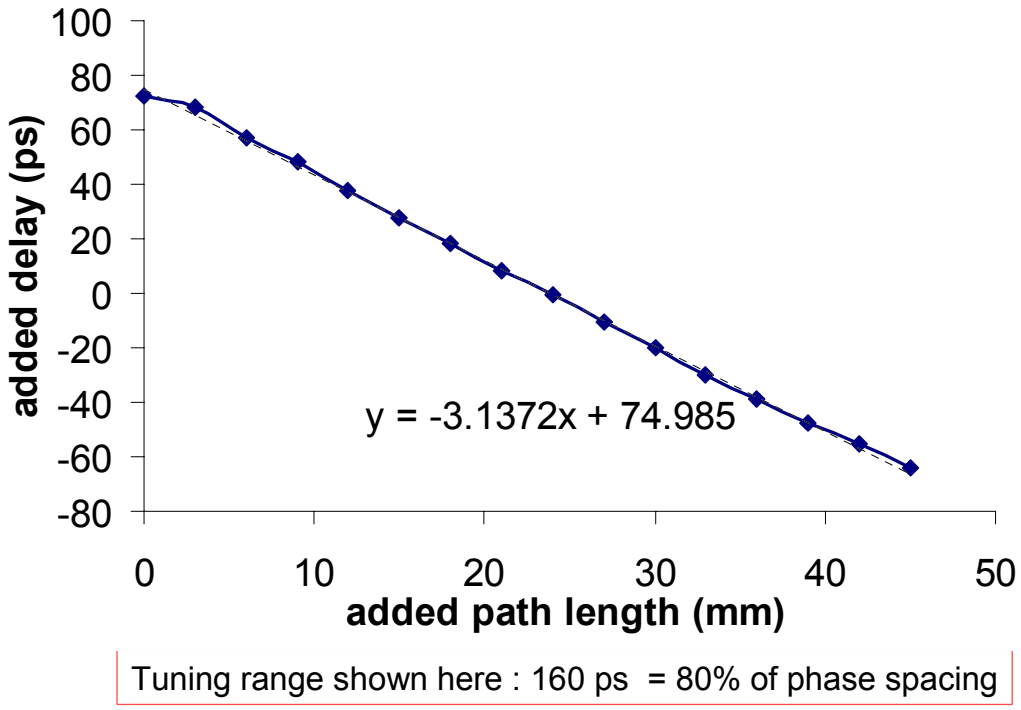



Figure 6.7 Plot of the tuning range for the clock phase. The phase spacing was adjusted by mechanically moving a corner cube on a translation stage

The low value of 1.74 ps electrical jitter may result from very careful design on a very quiet chip, and relies on direct electrical injection to the PLL from the precise external oscillator. In the optical case, the skew between adjacent phases was set precisely (as in Fig. 6.6), by adjusting delay by translating the corner cubes using the micrometers. Such precision was limited to two adjacent clock phases in the present optical setup. Fig. 6.7 shows that the range of delay adjustment was ~ 160 ps, limited by the alignment of the optical beams on the photo-detectors. The optical system is currently far from optimum, especially with the use of off-chip detectors and some vibration-sensitive bulk optics. The measurement here could potentially be improved by direct integration of the photo-detectors, which would eliminate the inductive slew limits from the bond wires.

It is useful to identify the major sources of jitter in the optical clocking experiment. Therefore, the pulse to pulse jitter of the mode-locked optical pulse-train was characterized. An optical cross-correlation experiment was performed where two adjacent pulses from the laser were made to overlap spatially on a non-linear optical element. To achieve this, the laser beam was split into two paths with a relative delay of one pulse period and made to overlap spatially on a doubling crystal. The second harmonic wavelength generated by the crystal was measured on a low speed photo-detector with sensitivity only at the second harmonic. The delay of one beam path was swept relative to the other to map out the cross-correlation of adjacent pulses in the pulse train (pulse-to-pulse jitter). To complete the measurement to determine the pulse-to-pulse jitter, the autocorrelation was also measured using the same procedure except with zero relative delay between the paths. The standard deviation of the pulse-to-pulse jitter was determined from these two measurements as:

$$\sigma_{\text{jitter}} = \sqrt{\sigma_{\text{cross}}^2 - \sigma_{\text{auto}}^2}$$

where $\sigma_{cross}$ and $\sigma_{auto}$ are the FWHM of the cross and auto-correlations respectively. The measured jitter values for the best and worst laser settings were ~ 120 fs and 350 fs with an error bar of +/-50 fs.[1] Hence, in an ideal optical clocking experiment a jitter ~ 0.1 – 0.2 ps rms should be possible, at least for pulse-to-pulse jitter. The data for these measurements is included in Appendix 6.1.

The specification for the jitter floor of the scope used for the measurement was 2.5 ps rms. However the actual jitter floor of the instrument was measured to be less. A square waveform from an Agilent 8133A pulse generator was used to simultaneously trigger the scope and provide an input to it. The input was routed through an electrical cable delay of ~ 23 ns so that the scope triggered with the same edge it was sampling. This eliminated the jitter of the pulse generator, yielding a measurement of the scope's internal jitter of 0.8 ps rms.

The measured jitter in the optical clocking experiment here was 0.93 ps rms. Subtracting 0.8 ps rms from 0.93 ps in quadrature yields that the jitter in the optical system was less than 0.5 ps. Similarly subtracting 0.8 ps in quadrature from the 1.73 ps rms for the electrical case yields 1.53 ps. Thus the electrical clocking represents a factor of three reduction in the jitter of the clock.

In conclusion, both electrical and optical communications require multiphase clocking to send data at high speeds. Optical clocks are a relatively easy addition to optical links if an appropriate short pulse source is available, and remove much of the multi-phase clock

[1] The auto-correlation also yielded the best and worst case pulse width of the laser to be ~ 150 fs and 270 fs.

generation, distribution and synchronization burden from the electrical domain while providing enhanced performance at high speed. These first experiments of picosecond optical clock distribution show proof of principle that such a distribution can have lower jitter than an electrical scheme. Precise mechanical control over clock phase was also shown to be achievable. In general, the use of short pulse lasers may allow clocks with excellent frequency stability and phase control, at least to a small number of points on a CMOS chip.

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# APPENDIX 6.1 Pulse-to-pulse Jitter Measurement for Modelocked Ti-Sapphire Laser using Optical Auto Correlation and Cross Correlation

The auto correlation and cross correlation full-width at half maximum pulse widths were measured and are tabulated below for a range of wavelengths and bandwidths. The autocorrelation and cross-correlation numbers are highlighted and the jitter numbers are boxed in the table. The temporal pulse width of the laser was calculated from the autocorrelation measurement by dividing by a fixed factor as tabulated. The shortest pulse width measured was ~ 150 fs and the corresponding lowest measured pulse-to-pulse jitter was ~ 114 fs.

The pulse-to-pulse jitter was calculated from the auto correlation and cross correlation data by subtracting them in quadrature. In these measurements, the laser had the maximum jitter when the pulse bandwidth was high, in the range of 10 nm or larger. The maximum measured pulse to pulse laser jitter was ~ 342 fs for a pulse bandwidth ~ 13 nm.

Table 6.1 Auto and cross correlation measurements for Spectra Physics' 'Tsunami' Ti:Sapphire short pulse laser

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| Center Wavelength (nm) | 830 | 830 | 830 | 830.03 | 832 | 833.86 | 834.16 | 834.52 | 837.04 |
| Bandwidth Laser (nm) | 7.6 | 9.6 | 11 | 15.24 | 13.04 | 11.08 | 9.8 | 6.72 | 6.63 |
| Repetition Rate (ns) | 12.44 | 12.44 | 12.44 | 12.444 | 12.441 | 12.433 | 12.429 | 12.42 | 12.401 |
| Autocorrelation FWHM (fs) | 246.64 | 233.37 | 266.66 | 313.294 | 286.62 | 273.15 | 260.01 | 266.62 | 259.48 |
| Sech^2 pulse factor | 0.6482 | 0.6482 | 0.6482 | 0.6482 | 0.6482 | 0.6482 | 0.6482 | 0.6482 | 0.6482 |
| FWHM: Pulse width [fs] | 159.872 | 151.27 | 172.849 | 203.077 | 185.787 | 177.056 | 168.538 | 172.823 | 168.195 |
| Cross-correlation width [fs] | 273.3 | 259.97 | 299.96 | 439.941 | 446.594 | 333.313 | 286.62 | 299.93 | 286.621 |
| std-dev of pulse to pulse jitter [fs] | 117.735 | 114.555 | 137.362 | 308.861 | 342.484 | 191.015 | 120.606 | 137.375 | 121.745 |

# Chapter 7

# Conclusions

As the speed of electronic circuits approaches 10 Gb/s and higher, the idea of bringing high speed optical signals directly to CMOS chips seems increasingly imminent. This convergence of electronic speeds with optical network speeds offers opportunities for using light to aid electrical functions in novel ways. For example, mode-locked lasers, which emit short optical pulses, have properties that can be exploited to improve the performance of link circuits in many ways. This dissertation explored low jitter optical clocking, which is one of several potential applications of mode-locked lasers in electronics.

## 7.1. Summary of Contributions

The essential electrical functions of clock generation and distribution have increased in complexity as chips have scaled to greater clock frequency. The primary figures of merit for a clock namely, skew, jitter, rise/fall time and power consumption might not be easily met in future designs. In this work the potential for optical clocking using mode-locked lasers to address the clocking problems of future electrical systems was investigated. This dissertation comprises the first demonstrations of the use of a mode-locked pulse train to deliver full-swing square wave clocks to CMOS chips with picosecond precision using integrated photo-detectors that directly drive the clock load. The major contributions and results were:

1) A receiver-less scheme, where a photo-detector directly drives the clock load without intervening receivers, was suggested and demonstrated experimentally [1]
    a) Receiver-less adds the least latency, electrical power consumption and area, but is limited in the number of distribution points for a fixed laser power budget.
    b) Within an optical power budget of 1 W, receiver-less clocking was estimated to be able to remove > 60 % of the clock latency for 1 – 10 GHz applications.
2) A quantitative model was developed to compare electrical and optical clock distribution and determine the benefits and areas of application for optical clocking[2]
    a) It was found that optical clock distribution can remove a significant fraction of the clock latency on a large chip resulting in lower jitter and skew. The number of injection points required for significant latency savings are practical and is ~ O(100).

b) Optical clock distribution, as envisaged, could lower the electrical power of a large chip by less than 30 %, requiring the lowest level of injection for the 30%.

c) Detector capacitance O(10 fF) is required for power efficient optical clocking.

d) In general given the optical power budget a smaller clock load can be clocked very precisely, or a large clock load can be clocked with less precision

3) This work included the first experimental demonstration of an optically clocked digital circuit using mode-locked lasers and integrated photo-detectors at 850 nm [3]

a) 30-50 fF detectors were achieved via chip-scale flip-chip bonding, and used to clock a small digital block resulting in an rms jitter of 2.8 ps at its output.

4) This work was the first to propose and investigate the use of blue short pulses for high speed CMOS photo-detection applications [4, 5]

a) The DC response of bulk and SOI CMOS detectors at 425 nm was measured. A 50 X improvement in response was observed over the 850 nm case.

b) Low jitter digital clocking of a small circuit was demonstrated with SOI CMOS detectors; however, detector response was lower than theoretically calculated and the effects of passivation and surface traps require further investigation.

5) Optical clock distribution to four points was used for a link transmitter application [6]

a) Sub-picosecond jitter was measured and a reduction of 3X over an electrical clock distribution was shown.

## 7.2. Future Work

Two areas of future work seem interesting and rich in possibility. One is a further study to improve the performance of CMOS photo-detectors and to make them smaller. A second area of work is to integrate and miniaturize more of the optical clocking system

and demonstrate a plausible form factor for computer application. This is presently potentially feasible due to the existence of compact research-level semiconductor and solid-state mode-locked lasers and integrated optics modules containing lithographically defined lenses, mirrors and splitters [7-9]

Regarding the first area of work, the speed and response of CMOS photo-detectors might be improved through a better understanding of the surface and dielectric properties. Thus further investigation of SOI and CMOS photo-detectors including smaller spacing detectors might allow optical clocking using these detectors to achieve the level of low jitter that has been measured for the laser.

Regarding the second area, optical clocking of more complex digital systems could be demonstrated in a compact manner by integration with planar optics substrates, such as those developed by J. Jahns et. al [9]. There is also potential for integrating cm sized mode-locked lasers on the same glass substrate or printed circuit board.

Further development of CMOS photo-detectors, and integrated optics, would be enablers for not only clocking but a variety of optical applications in electronics.

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